AccuCore

Simucad Sales Training

INTERNAL USE ONLY
NOT FOR CUSTOMERS

PDK TOKEN

SIMUCAD

Who Can Benefit Using AccuCore?

- Designers of High Speed Digital Chips Who Need To Verify Critical Timing of Blocks and Full Chips
- They Design The Following Types of Chips
  - Clock frequencies > 600 Mhz
    - Processors – Micro, Network, Embedded
    - Networking Chips – Ethernet, SONET (OC48, OC192)
    - DSP, micro-controllers
- They Use Aggressive Design Styles
  - Full Custom
    - All hand crafted transistor level design
  - Structured Custom
    - Some is Cell-based, Block-Based
    - Some may be Synthesized
- Their Designs Push the Limits of Traditional Gate Level Cell Library-based Static Timing Analysis

Challenges for Timing Analysis

- Complex design styles
  - Domino logic, DCVS (Differential Cascode Voltage Switch), Pass Transistor based, Fast Latches, etc.
  - Multiple clock schemes
- Accurate timing analysis
  - High Clock Frequency
- Large Design data base
  - Millions of Transistors, Rs and Cs
- Multi-level hierarchy
- Mixed design methodologies - multiple tools
  - Custom, Cell-based, Synthesized
- Numerous and frequent design changes

Existing Timing Solutions

- Custom Flow
  - Synopsys PathMill
    - All the blocks with PathMill
    - Full-chip with in-house tools
- Structured Custom Flow
  - PathMill, Synopsys PrimeTime, Cadence (Pearl, Ambit, Encounter)
    - PathMill at custom block level
    - PrimeTime for synthesized and top-level
  - Synopsys NanoTime
    - Recently announced with no customer feedback yet

Custom Flow – PathMill

- Strength
  - Most widely used Transistor-level STA
  - Well understood - capabilities, limitations and work-arounds
  - Well proven and correlated with silicon
- Weakness
  - Limited functionality and support
  - Reduced accuracy and reliability
  - Difficult to use
  - Lower performance

PathMill Limitations

1. Limited Functionality and Poor Support

- Hard coded circuit topologies
- Complex structures not supported
- Hard coded clock propagation rules
- Limited fixed set of timing checks
- Does not support full-chip – no budget constraints manager
- 10 year old technology with no support
- No new development
- Replaced by NanoTime at =<90nm

PathMill Limitations (cont'd)

2. Reduced Accuracy and Reliability

- Not accurate for shrinking feature size
  - Table look-up based transistor delay calculation
- Algorithm tuned for critical path analysis
  - Sub-critical paths are not guaranteed
- Delay based static Tsetup/Thold
  - Major timing risk
- Limited style of abstraction models

PathMill Limitations (cont'd)

3. Difficult to Use

- Complex set-up
- Requires vectors for simulating cells which are not hard coded in the tool
- Transistor level reports
- Flip Flop based design treated as latch-based
- Too Many False Paths
  - Path based on transistor directionality
  - No concept of function

PathMill Limitations (cont'd)

4. Lower Performance

- Each timing analysis run re-calculates delay resulting in significantly overall longer time to complete timing analysis
- Transistor based reports takes much longer to debug and analyze

Custom Flow – NanoTime

- Strength
  - Integration/calibration with PrimeTime, same delay calculator
  - Migration path/compatibility from Pathmill for =< 90nm
  - Part of NanoSim, HSIM, HSPICE, StarRC-XT bundle
  - SI - Automatic calculation of the delay impact caused by cross-talk
  - Support for Synopsys Design Constraints (SDC)
- Weakness
  - New unproven tool
  - Claims recognition of advanced circuits but this will take many years
  - Only accepts BSIM3 or BSIM4
  - Bi-directional devices must be manually checked
  - No table model constructs for custom cells

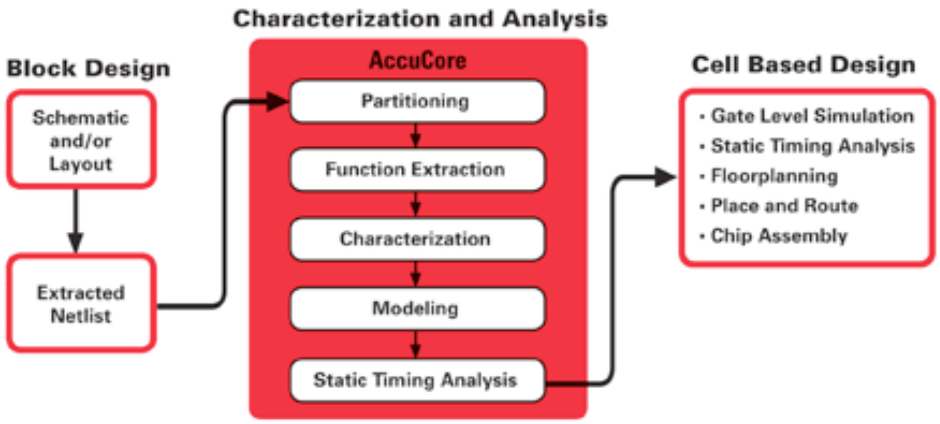
Structured Custom - PathMill/Primetime

- Strength
  - Offers full-chip timing flow
  - Industry standard, and proven
  - Well understood
- Weakness
  - Requires multiple tools integration thru scripting
    - PathMill, Delay Calculator, PrimeTime, custom scripts
  - Limits design methodology and accuracy
    - Multi-level hierarchical flow not supported
    - RC back-annotation
  - Long timing convergence cycle
    - PathMill ->RC extract->delay Cal->PrimeTime->ECO ->PathMill ->….

Traditional Gate Level Cell Library-based STA vs. In-Circuit Block Level Characterization and STA

- Limitations of Traditional Gate Level Cell Library-based STA
  - Long characterization time
    - **ALL** possible cells must be characterized under **ALL** possible output loads and **ALL** possible input slew conditions
    - Factor of N accuracy increase requires $\mathbf{N^2}$ simulation time increase
  - Accuracy losses
    - Table interpolation errors
    - Real-world non-linear effects **NOT** modeled
      - Piece Wise Linear (PWL) vs. actual stimulus, Miller Effects
    - Elmore RC delay model limitations
    - Ignores actual chip routing dependent RC effects
    - Ignores Well Proximity Effects (WPE)
    - Ignores chip level IR drop effects
- **Benefits of In-Circuit Block Level Characterization and STA**
  - Uses **actual** circuit loads, **actual** circuit slews and **actual** circuit RCs for both signal and supplies
  - **Rapid and accurate automated characterization with ALL in-circuit effects**

AccuCore – A New Paradigm



Full-Chip Transistor level characterization and Gate-Level Timing Analysis System

- Unified timing analysis tool for Custom and Structured Custom designs
- SPICE accurate dynamic characterization with automatic vector generation
- Multi-level hierarchy support
- High-capacity hierarchical static timing analysis
- Incremental capability for ECOs
- API for user customization

AccCore – Suited for Cutting-Edge Design Styles

- Algorithmic approach handles complex designs
  - Dominos
  - Fast latches
  - Pass transistor based logic
- Enables analysis of multiple clock domains

AccuCore – Ease-Of-Use

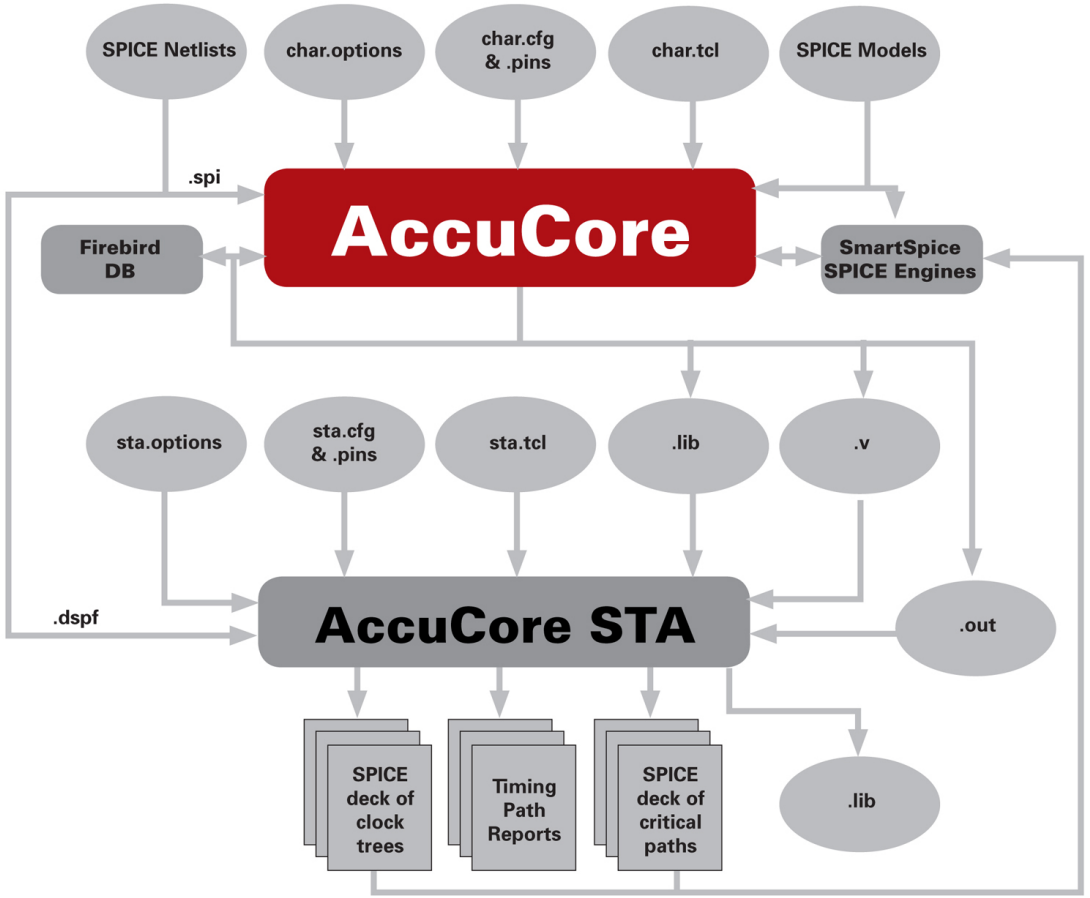
- Simple set up
- Flexible timing checks
- Clock propagation - user definable rule
- Removal of all local false paths - notion of function and vectors
- **Transistor-level STA with Gate-level ease-of-use**

AccuCore – Accuracy and Reliability

- AccuCore's "in-circuit" SPICE characterization, including Tsetup/ Thold
- Full coverage to guarantee critical, and sub-circuit paths
- Multiple abstraction models to support hierarchical analysis
- Critical Path SPICE simulation deck generated for inter-block paths
- Clock Tree SPICE simulation deck generated for inter-block paths

AccuCore – High Performance Timing Engine

- Multiple types of timing analysis on characterized data
- Incremental characterization for faster timing convergence
- Gate-level timing analysis - faster and easier
- Hierarchical timing analysis with multiple flow
  - Custom, Synthesized, DSPF, SDF

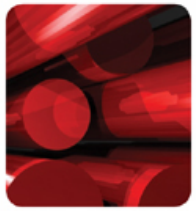


Customer Reasons For Change

- Current Solution Limitations
  - Extensive manual set-up
  - Limited functionality
  - Poor Support
  - Performance
  - Inaccurate
- AccuCore Solution
  - Simple to set-up
  - Easier usage model
  - Handles complex design styles - enables high performance
  - Dynamic characterization for SPICE accuracy and static gate level analysis for performance and ease-of-use
  - Incremental characterization for high throughput

AccuCore – Value for All Types of Customers

- Design Engineer Values
  - Time – complete analysis on schedule
  - Validation work is easier, more complete
- Senior Designer
  - Can use special circuit tricks to achieve performance
  - Tools can keep up with leading-edge design styles
- Manager
  - Meet design goals predictably, first time working silicon
  - Smaller staff required to validate design
- Director/VP
  - Beat competition by months, get design wins
- CFO – save 10 headcount, ROI, TTM, TTV



AccuCore Benefits

- **Accuracy**
  - Dynamic Simulation
  - Propagation of Slopes Tables throughout Design
- **Easy to use - Setup, Maintenance**
  - Automatic function extraction
  - Automatic Vector generation for Dynamic Simulation runs
  - No manual transistor direction setting
  - Simple configuration file
- **Supports aggressive design styles**
  - High performance designs - dynamic logic
- **Complex mixed level static timing analysis tool built in**
  - Critical Paths, Sub-critical paths, timing checks, Slack reports
  - SPICE deck creation of Critical paths (ready-to-run in SPICE simulations)
  - Various types of Model generation for hierarchical design and full-chip STA

Quicker timing convergence – Incremental characterization

Reduces Design Cycle

Improves Design Quality