Spider

Product Overview of
Place and Route Design Flow

PDK TOKEN

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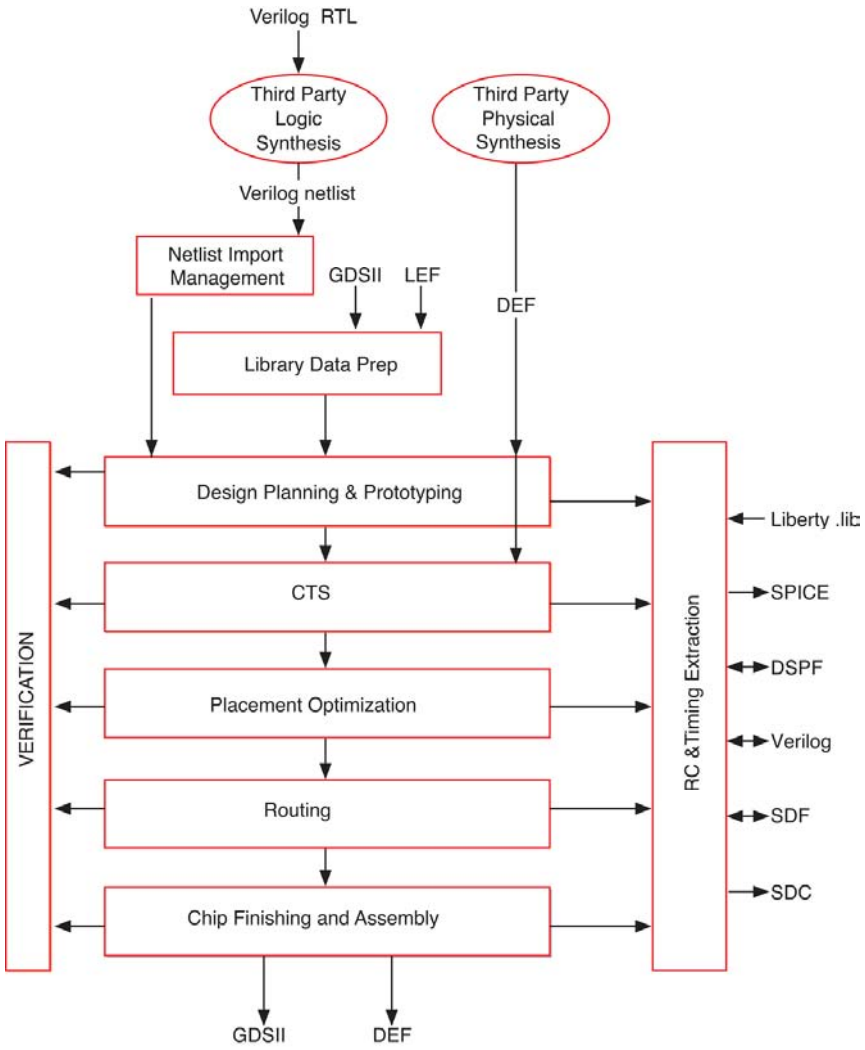
What is Spider?

- Spider is the industry's leading and affordable netlist-to-GDSII design environment, speeding concept to silicon
- Spider's advanced features enable:
  - Higher productivity
  - Faster turn-around-time
  - Eased design closure and
  - High quality of silicon
  - In a predictable fashion

Spider Inputs & Outputs

- LEF/DEF
- GDSII
- Verilog
- Liberty .lib
- SPICE
- DSPF



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Key Features

- **Physical Design Flow** with n-layer design capabilities ensures the expandability and flexibility needed to meet your tapeout requirements
- **Advanced Capabilities** enabled by the direct database system permits unrestricted "on-the-fly" review and editing of design data and parameters without requiring time-consuming data import and export format translation
- **Synthesis Support** integrates with third-party tools and legacy data through support for industry standard formats
- **Floorplanning with Mixed-Signal Support** within the toolset includes automatic placement and "what-if" analysis giving designers an early assessment of timing & area and providing predictable design closure
- **Placement Optimization** features like its automatic net-length minimization algorithms optimize cell placement
- **Automated CTS** features of Spider enable Clock Tree (CT) and High Fanout Net (HFN) Synthesis
- **130nm Routing** on cost effective server farms
- **RC & Timing Extraction** incorporating both embedded SPICE and RC extraction engines eliminating the need for external tools

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Physical Design Flow

- Physical layout with n-layer design capabilities
- User definable parameters with layout generation coding features
- Supports gate-array, structured-ASIC and standard-cell SoC design styles
- Facilitates control of every aspect of design process
- Highlight nets for review with ease

Advanced Capabilities

- The advanced direct database system permits unrestricted “on-the-fly” review and editing of design data and parameters without requiring time-consuming data import and export format translation.
- Self-Checking Correct-by-Construction Methodology
- Warns of potential problems without external post-process checking
- Dual GUI and command-line interface with “replay” log scripting for run-time automation

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Synthesis Support

- Integrates with third-party tools and legacy data through support for industry standard formats
- Imports verilog and EDIF netlist
- Liberty.lib timing library support
- LEF/DEF physical and technology library and design exchange format support

Floorplanning

- Automatic placement and “what-if” analysis
- Real-time netlist enforced layout and ECO processes assure error free connectivity control with on-line independent verification and correction utilities
- Built-in netlist, constraint, library and database checking and correction utilities assure valid place and route starting conditions and updates
- Automatic design partitioning
- Logical hierarchy netlist management
- Navigate and organize your design with advanced filtering and grouping options
- Padframe generation
- Chip and macro power planning and generation
- Automatic utilization estimation and aspect ratio control

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Floorplanning (cont'd)

- Support for multiple macro physical cell-types for easy "what-if" floorplanning analysis
- Placement and routing obstruction control features including rectilinear support for macros and regions with partial obstruction and overlap management
- Region controlled floorplanning
- GUI driven macro placement
- Displayed flylines during floorplanning allow you to place blocks to correctly minimize congestion
- Advanced visualization support permits viewing layout details at ANY desired detail or abstraction level with node highlighting

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Placement Optimization

- Automatic net-length minimization algorithms optimize cell placement
- 2D congestion map of placement
- Size and/or instance controlled clustering
- Programmable placement strategies permit mixed free-form and datapath-like cell placement methods

Automated CTS

- Enables Clock Tree (CT) and High Fanout Net (HFN) Synthesis
- Automatically optimizes insertion delay, skew and inter-clock skew
- Provides delay, transition, skew and load net details

Routing

- Performs automatic standard cell and padframe routing
- 130nm design rules support
- Real-time design rule enforced layout and ECO processes assure error free geometry design with on-line independent verification and correction utilities
- Mark specific nets for advanced automatic rip-up and re-route without needing to completely re-run placement and/or routing on the entire design or area
- Programmable automated contour, embedded block, ring, strap and rail routers make power and ground design and editing a breeze
- Easily perform interactive editing of either power and ground or signal nets with advanced placement and routing editors
- Snap, select, split, move, add corners and change layers during routing simply and quickly

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RC & Timing Extraction

- Embedded SPICE and RC extraction engines enable accurate and efficient post-route timing analysis including crosstalk effects

Easy to Use Solution

- Advanced physical view modeling and checking support
- Easy “what-if” floorplanning analysis capabilities
- Automatic layout generators
- Powerful UPI and scripting lets you create macros and advanced custom automation environments
- Macro automation to simplify repetitive tasks
- Easily replace cells and update the netlist at any time in the design flow
- Simplified top-level assembly and planning with automatic object snapping (gravity)
- Perform select, shift, move, rotate, flip, mirror and cell physical-type operations and edits with ease

Summary

Complete Physical Design Flow

- Complete physical layout with n-layer design capabilities ensures the expandability and flexibility needed to meet your tapeout requirements
- Advance user definable parameters and layout generation coding features ensure the ease and flexibility required to complete complex design and chip finishing tasks
- Optimization happens throughout the flow (i.e placement, CTS, route)
- Supports today's demanding IC designs with physical design tools that maximize efficiency
- Supports gate-array, structured-ASIC and standard-cell SoC design styles
- Facilitates control of every aspect of design process
- Perform Engineering Change Orders (ECOs) and highlight nets for review with ease

Advanced Capabilities

- The advanced direct database Graphical Engineering Access Routines Scripting (GEARS) system permits unrestricted querying and editing of design data and parameters for "on-the-fly" inspection and correction without requiring time-consuming data import and export format translation
- Self-Checking Correct-by-Construction Methodology
- Supports physical synthesis methods
- Built-in cross-talk extraction and reporting warns of potential problems without external post-process checking
- Very accurate full-chip multi-threaded 2.5D parallel RC netlist extraction for post-route sign-off timing, power and noise/SI checks
- GUI and command-line interface with "replay" log scripting for run-time automation

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