Abstract

Single-Event Gate-Rupture (SEGR) in Vertical Double Diffused Metal-Oxide Semiconductor (VDMOS) power transistors exposed to a given heavy ion LET occurs at a critical gate bias that depends on the applied drain bias. A method of predicting the critical gate bias for non-zero drain biases is presented. The method requires as input the critical gate bias vs. LET for $V_{DS} = 0V$. The method also predicts SEGR sensitivity to improve for larger gate-oxide thicknesses. All predictions show agreement with experimental test data.

Introduction

Single-Event Gate-Rupture can lead to power MOSFET failure in space. The SEGR process is initiated when a heavy ion strikes the device in the neck region. The neck region is the area between the p-body diffusions at the surface (see Figure 1). The ion strike creates a filament of electron-hole pairs. For an n-channel power MOSFET, the generated holes drift toward the interface and the electrons toward the drain contact due to the electric field resulting from the positive drain bias. Upon reaching the interface, the holes start to ‘pile up’ at the interface and ‘leak off’, only slowly, toward the source contact. This pool of positive charge increases the electric field in the oxide, and when the field exceeds a critical value, oxide breakdown occurs. The collected holes then discharge through the oxide, heating the structure locally. If the breakdown current lasts long enough, a permanent short-circuit through the oxide results.

While progress has been made in empirically describing SEGR and modeling the mechanism [1]-[5], its dependence on structural parameters has not been elucidated. In this work, a simple model that utilizes two-dimensional ATLAS simulations to predict SEGR breakdown condition for a given heavy ion LET is introduced. The predictions were used to investigate SEGR dependence on oxide thickness, LET of the incident ion, and the $V_{GS}$ versus $V_{DS}$ interrelation at rupture. A "base-line" cross section of the devices used in the 2-D simulations and in the experiments is illustrated in Figure 1. Device details for the simulated VDMOS transistors were based on SSUPREM4 profiles for stripe geometry test structures that were built for experimental verification of oxide thickness dependence. The experimental data are reported fully elsewhere[3]. The following sections will further discuss the SEGR mechanism, present a methodology for predicting SEGR, and illustrate the excellent agreement between the prediction technique and experiment.

Prediction Methodology

In order to evaluate SEGR hardness of power DMOS transistors, it is common practice to find the threshold biasing condition in a given radiation environment (LET of incident ion given). Operating a DMOS device below this threshold biasing conditions ($V_{DS}$, $V_{GS}$) guarantees safe operation whereas exceeding this threshold will result in gate rupture and, thus, destroy the DMOS transistor. One method to find these threshold biasing conditions is an experimental approach (see [2], [3]). However, these experiments are usually rather costly and time consuming. In this paper, we will show an alternative method to derive these threshold bias conditions by combining a fast and inexpensive prediction algorithm that utilizes 2-D simulation results (PISES...
simulations) with measured oxide breakdown strength $E_{cr}$ vs. LET data for $V_{DS} = 0\text{V}$. The method is based upon

$$V_{GS\text{cr}} = d_{OX} \times (E_{cr} - E_{trmax}) \quad (1)$$

where $V_{GS} = \text{critical gate-to-source bias for SEGR}$, $E_{trmax}$ = maximum transient oxide field from 2-D simulation for $V_{DS} = 0$, $E_{cr}$ = experimental input for $V_{DS} = 0$, and $d_{OX}$ = oxide thickness. Each of these components is now to be described in detail.

**Modeling the Transient Oxide Field ($V_{DS} \neq 0$)**

SEGR dependence on LET, gate-oxide thickness, and $V_{GS}$ versus $V_{DS}$ interrelation in VDMOS n-channel power transistors was investigated through 2-D simulations. For all simulations, the ion was assumed to traverse the device at normal incidence through the center of the neck region. In the simulations, we used cylindrical geometry and generated the charge due to the passing energetic ion as a charge cylinder with a Gaussian lateral distribution of characteristic length $L = 0.07\mu\text{m}$ and uniform distribution in depth. Details of the simulation of the ion track are given in the Appendix.

An example of the transient oxide field obtained from 2-D simulations is shown in Figure 2. Input data supplied by a user for the simulation includes structural dimensions of the test device, energy and spatial information of a traversing ion, and bias conditions for the device. The simulator then computes various physical quantities including potential distribution, electric fields, and carrier concentration profiles. The result of practical interest is a critical transient condition for a VDMOS device that leads to SEGR (for a given LET value of the incident ion). A difficulty in applying our 2-D simulation results is that no oxide breakdown model is included in the simulations. We now describe how we have dealt with this problem.

If we assume the total charge generated in the oxide is small compared to the filament charge in the silicon, then the electric field in the oxide is the sum of a transient field component due to substrate charge collection effects (related to $V_{DS}$ [1]) plus a DC field component due to $V_{GS}$ (see equation (2))

$$E(t) = E_{cr}(t) + E_{DC} \quad (2)$$

The DC part of the oxide field $E_{DC}$ can be calculated with the simulator for any given biasing condition when there is no ion strike (zero charge generation). $E_{DC}$ is approximately (neglecting work function differences)

$$E_{DC} \approx |V_{GS}|/d_{ox} \quad (3)$$

For sufficiently negative $V_{GS}$ values (in n-channel devices), there is no dependence of $E_{DC}$ on $V_{DS}$ because the surface is inverted and the inversion layer places the Si/SiO$_2$-interface on the same equipotential as the grounded body contact [4]. The simulated transient component of the oxide field, $E_{cr}$, reaches its peak value within a few pico seconds after the charges due to the traversing ion are generated (see for example Figure 2). The transient field persists for a time of about 50ps which varies somewhat with LET and $V_{DS}$.

One might expect that oxide transients of such short duration would not be as fully effective as a DC oxide field in causing SEGR. However, comparison of 2-D simulations at biasing conditions where SEGR was detected experimentally with experimental results indicated that failure occurs when the transient oxide field exceeds a critical value, $E_{cr}$, made up of any combination of DC and transient components.

Using equation (5) for the LET-dependence of $E_{cr}$ and the empirical assumption that transient and DC oxide field contribute on the same basis to $E_{cr}$ it is simple to predict a critical gate-to-source bias $V_{GS\text{cr}} = V_{GS}$, that initiates SEGR for a given heavy ion LET and a given drain-to-source bias $V_{DS} > 0$.

**DC Input Data ($V_{DS} = 0$)**

For DC applied fields and for normal incidence of the ion, Wrobel [5] measured the dependence of $E_{cr}$ on the ion’s LET value. Equation (4) is Wrobel’s empirical fit to experimental breakdown data on heavy-ion irradiated MOS-capacitors,

$$E_{cr} = 40.8 \frac{1}{\sqrt{LET}} \quad (4)$$

where LET is in MeV cm$^2$/mg and $E_{cr}$ is in MV/cm. This fitting function is inaccurate for low LET values where it predicts that $E_{cr}$ is infinite as the LET value ap-
proaches zero. A better fit to the data that agrees with
the intrinsic breakdown value of $E_{cr} = E_0$ for LET values
of the incident ion approaching zero is,

$$E_{cr} = \frac{E_0}{1 + \text{LET}/B}$$

(5)

where LET and B is in MeV cm$^2$/mg and $E_{cr}$ and $E_0$
is in MV/cm. It is usually very difficult to measure the
intrinsic breakdown field of a gate-oxide (LET=0) using
MOS devices because the oxide usually tends to break
down at a lower field strength at a defect related weak
spot of the oxide. The breakdown location for irradiated
oxides, on the other hand, will be at the strike location
that usually does not coincide with a weak spot of the
oxide. Therefore, to extract dielectric breakdown data
of the gate-oxide ($E_{cr}$ vs. LET), the breakdown field for
LET=0 will not be measured but extrapolated by fitting
expression (5) through the experimental data points for
LET>0. Applying this procedure to Wrobel’s [5] exper-
imental breakdown data yields $E_0 = 11.1$ MV/cm and $B$
= 62.1 MeV cm$^2$/mg. The breakdown strength of differ-
ent oxides varies somewhat due to different processing
steps, and is a necessary input for our prediction algo-
rithm. The solid line in Figure 3 was obtained by fitting
equation (5) to the breakdown data for the devices used
in this work $E_0 = 9.1$ MV/cm, $B = 58.0$ MeV cm$^2$/mg) The
symbols in Figure 3 correspond to experimental data
points taken from the stripe line geometry DMOS tran-
sistors used in this work.

$$1/E_{cr} = 9.08/(1 + \text{LET}/58.04)$$

Figure 3. Inverse breakdown field due to applied gate-to-
source bias $V_{GS}$ versus LET of the incident ion. Symbols show
experimental data on irradiated devices with $V_{GS}=0$ and solid
line was obtained by a least square fit of expression (5) to
devices with various oxide thicknesses.

Outline of Method

Below, an outline is given that shows how to obtain a
prediction for the maximum (critical) gate-to-source bias
$V_{GS}$ that can be applied to a VDMOS power transis-
tor for a given heavy ion LET with a specified drain-to-
source bias $V_{DS} \geq 0$. Exceeding this critical bias $V_{GS}$ will
initiate SEGR and cause destruction of the device.

1. Define input deck for 2-D simulator ATLAS including:
   - device geometry and dimensions.
   - drain-to-source bias, $V_{DS} > 0$, where correspond-
ing critical gate-to-source bias, $V_{GS}$, is sought.
   - input parameters for charge distribution along the ion
     track (apply equations (A7)-(A10) shown in Appendix).
   - arbitrary negative gate-to-source bias, $V_{GS}$, suffi-
cient to invert the surface (The transient portion of
   the oxide field due to substrate charge separation
   computed below does not depend on the choice of
   $V_{GS}$ at this point.)

2. Run ATLAS
   - find the DC field component $E_{DC}$ (LET=0).
   - initiate charge filament appropriate to the ion LET
     along ion strike path and continue with a transient
     simulation to compute oxide field versus time at
     the strike location.
   - extract the peak field magnitude $E_{p}$.

3. Compute peak magnitude of transient oxide field
   component (at given drain-to-source bias $V_{DS}$)

$$E_{p} = E_{DC} - E_{p}$$

(6)

4. Compute critical oxide field $E_{cr}$ for given LET of inci-
dent ion from equation (5).

5. Compute critical gate-to-source bias, $V_{GS}$ for given
   $V_{DS}$ and LET) with equation 1.

Simulation Results

Four different gate oxide thicknesses ranging from 50nm
to 150nm as used in the experiments [3] were simulated.
For every change in oxide thickness, the structure under-
neath the Si/SiO$_2$ interface was left unchanged and only
the thickness of the gate-oxide was adjusted to the desired
value. The drain bias $V_{DS}$ was held at a bias of interest and
the arbitrary value of the gate-to-source bias $V_{GS}$ was
chosen between -6.5V and -28.5V (sufficiently negative to in-
vert surface prior to the ion strike). Simulations were per-
formed for three different incident ions (i.e., Nickel (LET
= 26.6 MeV cm$^2$/mg), Bromine (LET = 37.2 MeV cm$^2$/mg),
and Gold (LET = 82 MeV cm$^2$/mg)) and for all the various
oxide thicknesses the critical oxide breakdown strength
was taken from the data shown in Figure 3. Figure 4 shows
four snapshots from the transient simulation to illustrate
the spacial migration of the charge filament in time.

Comparison of Predictions
with Experiments

All experiments were performed at the Brookhaven Na-
tional Laboratories (BNL) tandem Van de Graaff facility
and are reported fully elsewhere [3]. Figure 5 shows the
threshold biases $V_{DS}$ and $V_{GS}$ for a bromine incident ion. The symbols in Figure 5 show experimental data points for five different gate-oxide thicknesses ranging from 50nm to 150nm. The solid lines in Figure 5 were obtained with our prediction algorithm. The predicted threshold biases are in excellent agreement with experimental data for all oxide thicknesses investigated in this work. Figure 6 shows the threshold biases $V_{GS}$ at a drain bias of $V_{DS}=30V$ as a function of LET to further verify the usefulness and potential of this prediction algorithm. Again, the predictions are in excellent agreement with experiments for all three different gate-oxide thicknesses.

**Conclusion**

A simple prediction method for SEGR using a 2-D device simulator was presented. This prediction method utilizes oxide breakdown information (i.e. SEGR data for $V_{DS}=0$) to predict critical rupture biases ($V_{GS}$, $V_{DS}$) for a given heavy ion LET on devices operated at a nonzero drain-to-source bias (i.e. $V_{DS}>0$ for n-channel device). Prediction results showing critical threshold conditions to initiate SEGR in DMOS power transistors are in excellent agreement with experimental data. The observed dependence of SEGR on $V_{GS}$ versus $V_{DS}$, gate-oxide thickness, and the LET value of the incident ion confirm the prediction algorithm.

**Appendix**

Equation (A7) shows the mathematical form of the charge distribution, with $r =$ radial direction, where $r = 0$ corresponds to the center of the track/neck region. Expressions (A8)—(A10) were used to calculate the carrier concentration per unit volume $N_0$ at the track center [7]. The charge distribution of the track is generated uniformly in depth. A more accurate representation of the charge generation along the ion track could be obtained by taking the energy loss of the ion along its path through the device into account. However, exten-
sive 2-D simulations have shown that only the charges generated in approximately the first micron from the Si-SiO$_2$-interface contribute to the collected holes that raise the oxide field.

$$N(x) = N_0 \exp \left\{ - \left( \frac{x}{L} \right)^2 \right\}$$  \hspace{1cm} (A7)

$$N^i = \int_0^r rN_0 \exp \left\{ - \left( \frac{r}{L} \right)^2 \right\} dr = N_0 \pi r^2$$  \hspace{1cm} (A8)

$$N^i = \frac{LET[MeV cm^2/mg]}{3.6[eV/pair]} \times 2.33[gm/cm^3] \times 10^2$$  \hspace{1cm} (A9)

$$N_0 = \frac{N^i}{\pi L^2}$$  \hspace{1cm} (A10)

The charge column due to the traversing heavy ion was ramped up to its final value over a short time interval, $t_0=1fs$. This was achieved by increasing the carrier generation rate constant locally in the track region and running a transient simulation up to $t=t_0$. For $t > t_0$, no further pair generation is allowed, and the electron/hole transport in the substrate is modeled using ATLAS.

References


Notes

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