MixedMode Simulation of Power Electronic Converters

M. Trivedi, A. Mulay, R. Vijayalakshmi, and K. Shenai
Department of Electrical Engineering & Computer Science, 1135 SED
University of Illinois at Chicago,, Chicago, IL 60607

Introduction

With mounting concern for energy conservation and nature preservation, power electronics is becoming increasingly dominant in everyday life. Power electronics systems have proliferated to a wide range of applications from telecommunications and information processing to medicine and transportation. Radical developments in power semiconductor devices have been instrumental in this power electronics revolution.

In order to push the technology further, new device structures and process technologies are rapidly being developed. Complexity of these device structures and processes hinders a full understanding of device operation based on the structural information alone. Improper understanding hampers the development of reliable circuit models of these circuits. It is essential to understand internal carrier dynamics for optimum utilization of a high power device.

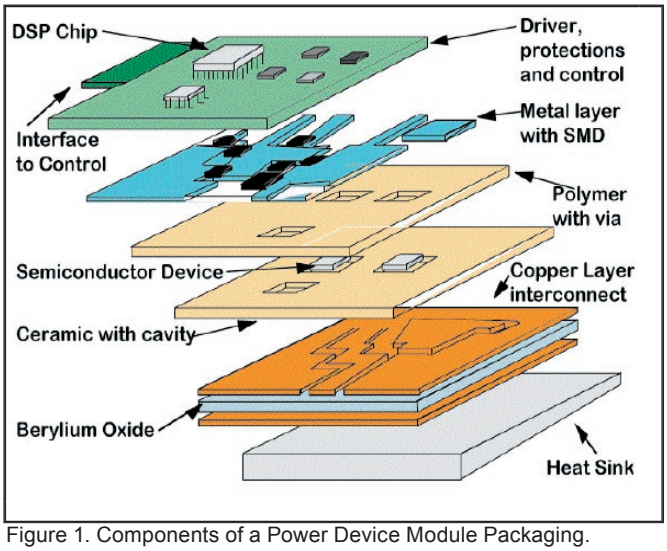

Figure 1. Components of a Power Device Module Packaging.

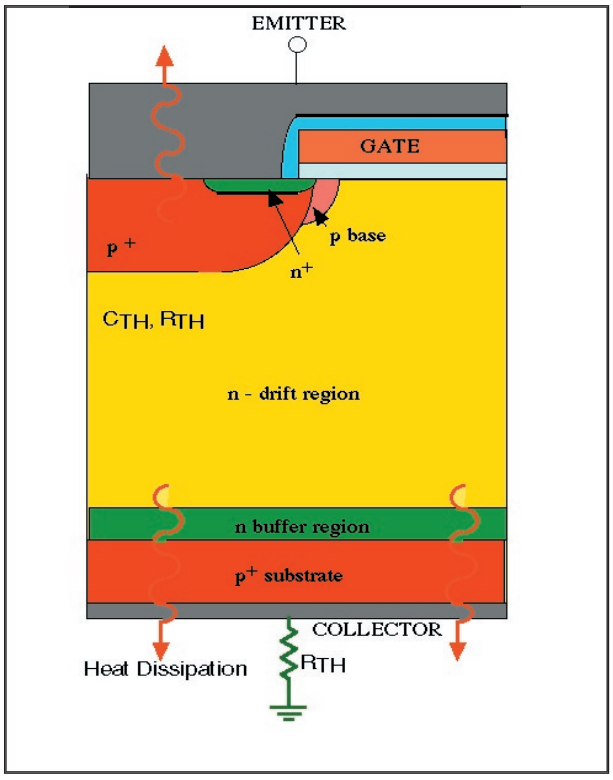

Figure 2. Two-dimensional representation of Insulated Gate Bipolar Transistor along with thermal resistance at collector electrode.

Power semiconductor devices are mostly used in applications that subject them to high stress conditions. Some such conditions include short circuit and inductive load turn-off. The device has to conduct rated current with bus voltage across its terminals in such conditions. Large power dissipation results in considerable heat generation within the device. Thermal considerations can seriously compromise device reliability, and, in fact, limit the Safe Operating Area (SOA) of the device at the high-voltage, high-current limit. Efficient heat dissipation becomes an important issue as the power device module becomes more complex to cater to a greater demand for application specific system solution. Various layers in a typical Application-Specific Power Electronics Module (ASPEM) are shown in Figure 1. Heat generated within the device diffuses through the semiconductor and various packaging layers before being dissipated in the ambient. Thermal resistance of the package should be very low to facilitate better heat dissipation. Further, the wire bonds may fail at high temperature levels. A better understanding of electrothermal performance of the device will lead to development of more reliable devices and more efficient package designs.

Traditionally, device optimization involves running split-lots in a wafer fab, and measuring the electrical characteristics of prototype devices. This is a very expensive and time-consuming venture, especially so as wafer sizes increase and processing equipment becomes

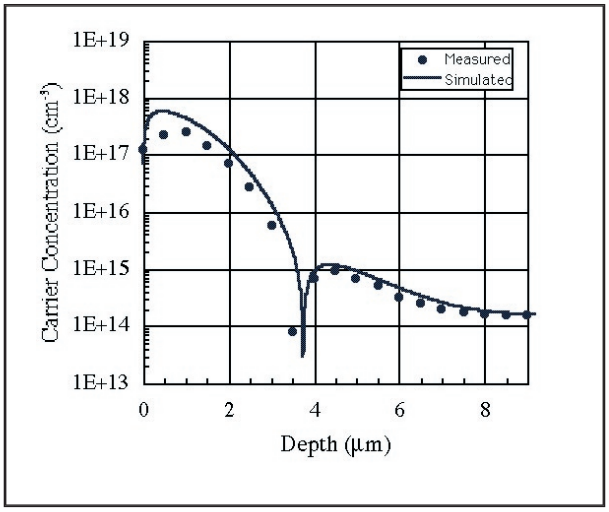

Figure 3. Measured and simulated doping profile of the p-base of IGBT.

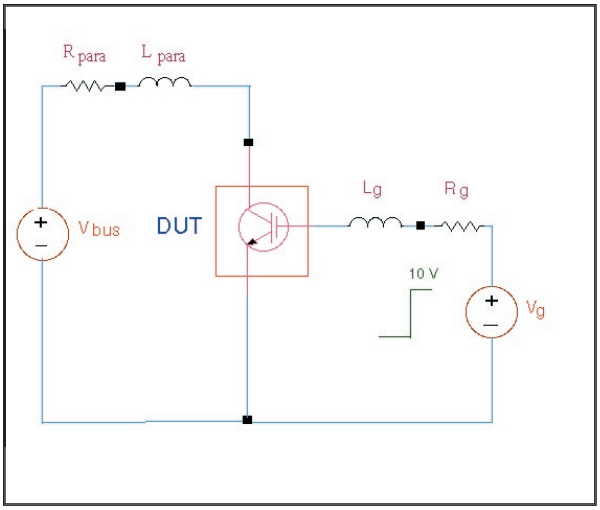

Figure 4. Test circuit used for short-circut switching study.

more expensive. Two-dimensional numerical simulators are emerging as invaluable tools towards a better understanding of semiconductor device dynamics under actual circuit conditions [1]. By solving semiconductor equations at each point within a 2-D representation of the device, under boundary conditions imposed by external circuit elements, 2-D simulators provide direct access to internal device parameters. This enables optimization of device carrier dynamics in an actual circuit application environment. Electrothermal simulations can be performed to incorporate effects of self-heating that results from power dissipation within the device. Package influence can be accounted for by connecting thermal resistance of various layers, as depicted in Figure 2 for an Insulated Gate Bipolar Transistor.

Simulation of Power Converters

In this paper, the importance of mixed-mode simulations is demonstrated in the study of Safe Operating Area of Insulated Gate Bipolar Transistors (IGBT) [2]. The cross-section of the device, shown in Figure 2, was created from the process flow using the two-dimensional process simulator ***ATHENA*** [3]. The device is rated 600 V, 50 A. Simulated doping profile of the p-base is compared with SRP data in Figure 3, revealing a very close match between the two doping profiles. Effective area and lifetime of the device were determined to obtain a good match with measured static characteristics. Matching of static characteristic was done using the 2-D device simulator, ***S-Pisces*** [4].

The structure generated was then used in the mixed device and circuit simulator, ***MixedMode***[4], to perform electrothermal simulation of short circuit performance of the device. In many power conversion applications, short circuit condition is a frequently occurring fault. Ability of the power device to withstand short circuit conditions is an important requirement. The test circuit used for the study is shown in Figure 4. Influence of the package is accounted for by attaching thermal resistance of various packaging layers at the device electrodes. Thermal boundary conditions were applied by maintaining the device electrodes at an ambient temperature of 400 K. Performance of the device under short circuit stress of 10μs is shown in Figure 5. When the device is turned on initially, current increases rapidly, but then starts drooping. This results from mobility reduction due to temperature rise. The device successfully turns-off after 10μs of stress. Extended exposure of the device to this condition eventually leads to device failure, as shown in Figure 5, by the dashed lines. After breakdown, device current rises rapidly and uncontrollably, while voltage falls down [5].

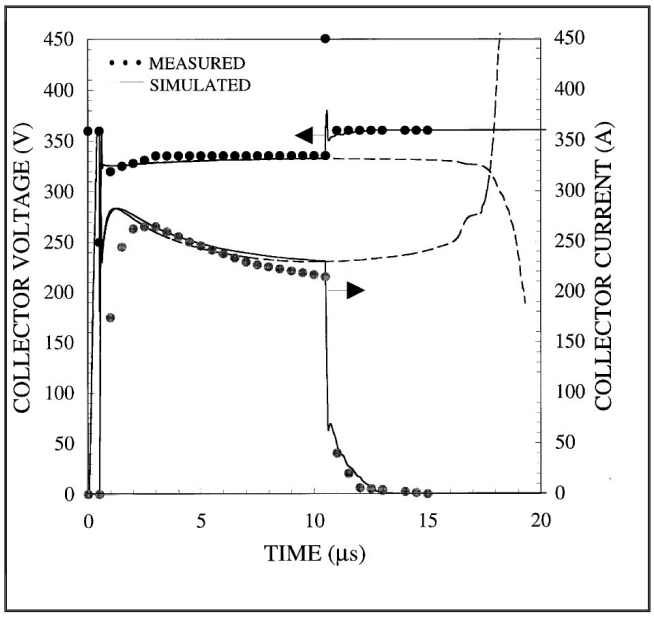

Figure 5. Measured and simulated short circuit performance of IGBT.

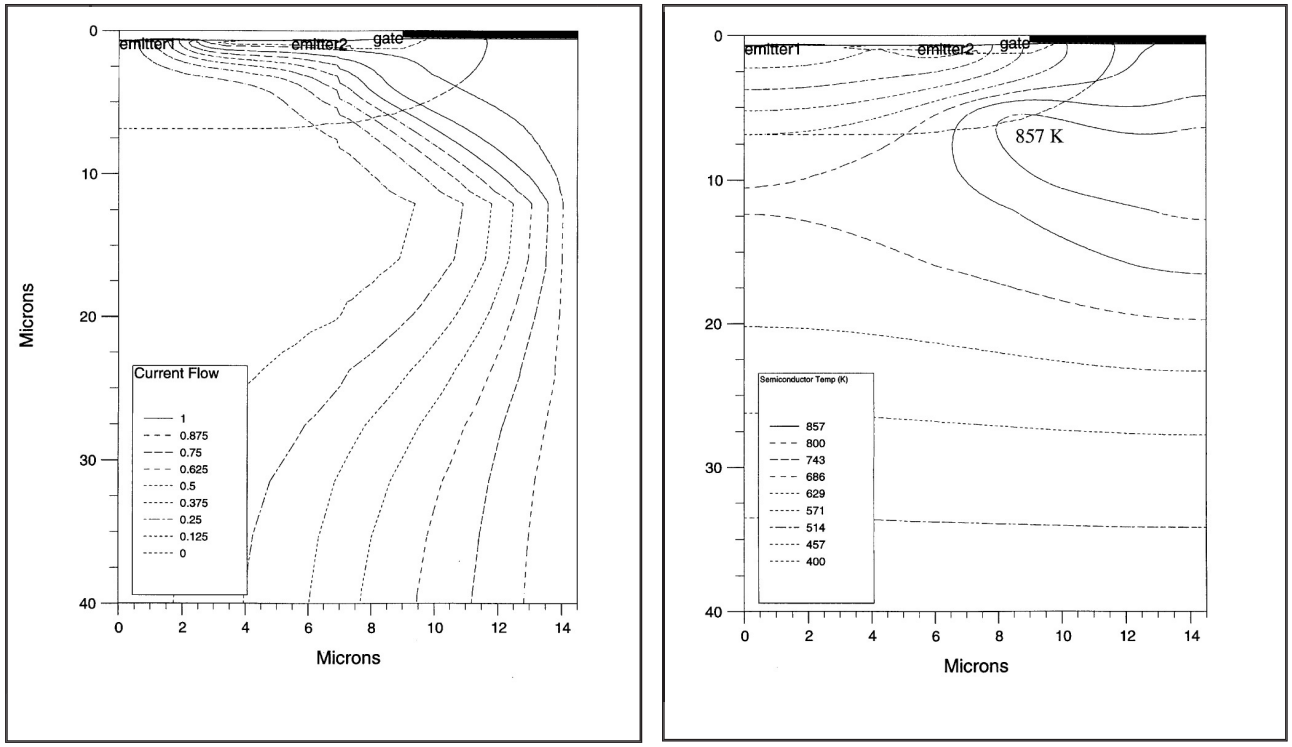

Figure 6. (left) Current flowlines, and (right) temperature distribution within the device at short circuit failure.

Figure 6 depicts the current flowlines and temperature distribution within the semiconductor for the device conducting in breakdown condition. As can be seen in Figure 6, current flowlines are concentrated at the curvature of the p-base n-drift region junction. Maximum temperature within the device is localized in the same region, as shown in Figure 6. the reverse biased p-base n-drift region supports the entire applied voltage leading to a significant electric field. High current density through the region leads to significant power dissipation and temperature rise. At higher temperatures, there is an increased availability of carriers. This leads to a further increase in the impact generation rate in the high field region. Impact generation in this region and temperature rise initiate a regenerative process and the device finally breaks down due to thermal instability [5]. Location of the hot spot was confirmed experimentally using IR imaging techniques.

With an understanding of the physical phenomena governing the observed characteristics, mixed device and circuit simulations can be used to make changes in actual process and device design parameters. These changes can significantly impact both performance and Safe Operating Area (SOA) of the device. Important trade-off among performance and SOA parameters can be identified, and traded-off using the ***ATHENA*** and **ATLAS** frameworks at process and device level.

Conclusion

As power semiconductor devices find more widespread and multifarious use in industry, it is becoming important to design and optimize the devices at the application level. Mixed device and circuit simulations offer an economical, feasible and competitive alternative to running several split lots in the wafer fab for application-specific optimization of devices. ***ATHENA*** and ***ATLAS*** frameworks have been successfully used in this work to study the short circuit failure of IGBTs. Electrothermal simulations allow study of the effect of self heating on circuit performance of the device. The simulator also incorporates electrical and thermal package parasitics.

References

[1] K. Shenai, "Mixed-mode circuit simulation: an emerging CAD tool for the design and optimization of power semiconductor devices and circuits," IEEE 1994 PELS Workshop on Computers in Power Electronics, 1994, pp. 11-15

[2] M. Trivedi and K. Shenai, "Mixed-mode simulations for power system optimization," 21st Intl. Conf. on Microelectronics, 1997, pp. 451-458

[3] ATHENA Users Manual, Silvaco International, Santa Clara

[4] ATLAS Users Manual, Silvaco International, Santa Clara

[5] M. Trivedi and K. Shenai, "Investigation of the Short-Circuit Performance of IGBTs," IEEE Trans. Electron Devices, vol 45, no. 1, pp. 313-320, 1998.