Low-Power Systems-on-a-Chip CAD

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Introduction

Mixed-signal systems-on-a-chip (SOC) integration of digital, analog, RF, and power components is emerging to meet demands for low-power, highly integrated systems in portable computing, wireless communications, and multimedia. Applications are also found in transportation [1] and in aerospace/defense. Lithography scaling trends are fueling this development, with RF performance now possible from bulk CMOS. Deep submicron devices, however, are increasingly sensitive to second-order effects with the result that traditional circuit simulations cannot accurately predict performance without first accounting for specific device structures and layout topography. The complex interaction between digital switching logic and analog or RF continuous wave circuits further complicates simulation and modeling. Described below are the tools necessary for SOC design and modeling, as well as two applications examples based on research being conducted at the Systems on Silicon Research Center (SYSREC) at the University of Illinois at Chicago (UIC).

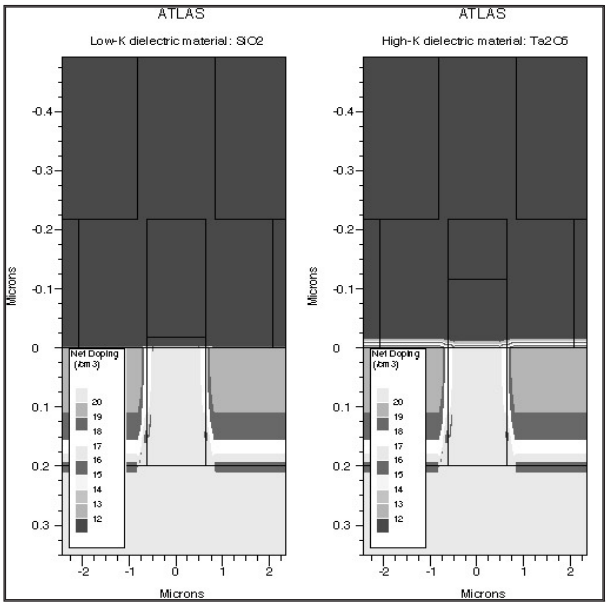

Figure 1. Device structures constructed in DEVEDIT for an NMOSFET comparing S_iO_2 and Ta_2O_5 gate dielectric materials.

Simulation

For device fabrication, numerical simulation of processing steps with ***ATHENA*** results in structures which more closely match manufactured devices than is possible using assumptions of ideal processing. The structures produced from process simulation are critical to evaluating device reliability and predicting sensitivity to process variation. For example, the electric field distribution in deep submicron devices at the edges of the drain region determines avalanche breakdown characteristics. Accurate doping profiles, reflecting impurity redistribution following subsequent thermal processing steps, are needed instead of idealized profiles to reveal failure sites within the device. Doping redistribution in the channel region has also been shown to influence short-channel effects. In deep submicron devices, channel carrier quantization possibly violates drift-diffusion physics, and simulation of these quantum effects rely on precise impurity locations.

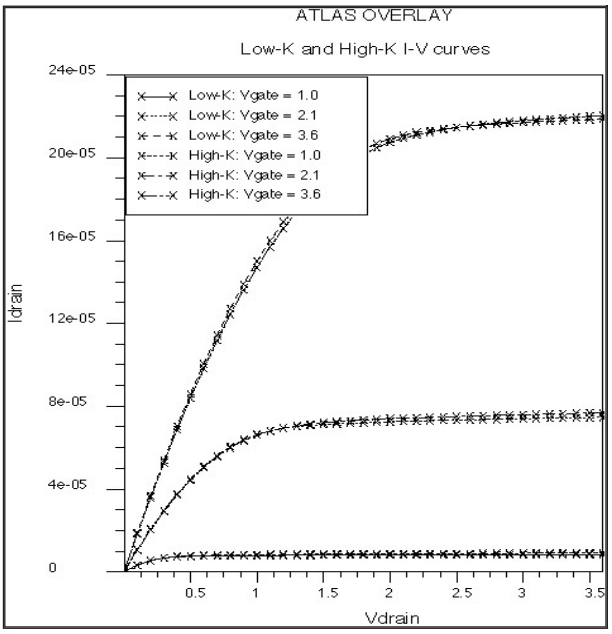

Figure 2. I_D-V_{DS} comparison of high-K gate dieletrics versus conventional processing. The high K material allows equal drive current with a thicker dielectric.

As devices are scaled down to deep submicron dimensions and are operated at frequencies extending into gigahertz, existing circuit models fail to predict capacitive behavior and cannot account for internal heating due to dynamic switching activity. Numerical simulation, particularly RF numerical simulation, is necessary to capture non-isothermal high-frequency switching performance. Scaling also introduces a number of reliability issues not accounted for in traditional transistor models. In devices with an effective channel length approaching 0.1 micron, a gate oxide of under 40 angstroms is required. The device robustness is degraded, since oxide tunneling is increased and defects critically affect the lifespan of the dielectric. To address these shortcomings, new high dielectric constant materials are being considered to provide the same gate capacitance using a thicker material. Device numerical simulation

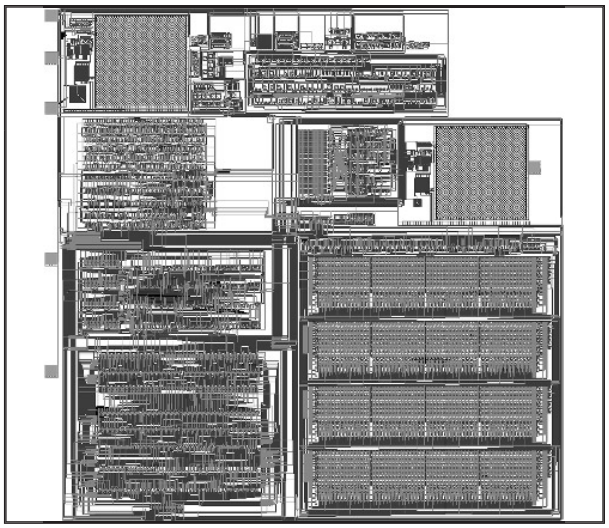

Figure 3. System-on-a-chip layout from UIC.

is required to assess the impact of thin and thick dielectric materials on first-order characteristics like I-V and C-V curves, but more importantly, second-order effects like breakdown and gate control of the inversion layer. Figure 1 shows the structures, created in DevEdit, of an NMOSFET using S_iO_2 and Ta_2O_5, respectively, as a gate dielectric. Simulation results from ***ATLAS***, shown in Figure 2, confirm a match in the I-V curves. Further work is being performed to develop device structures for low- and high-dielectric constant gate oxides for RF applications. ***ATLAS*** is used in optimizing the output characteristics and relate process parameters to specific performance criteria. ***ATLAS*** has been applied previously to evaluate self-heating effects in silicon-on-insulator CMOS [2] and in the modeling of power MOSFETs for RF applications [3].

In designing a complete SOC, analysis of the signal delays and impedances of global and local interconnects is necessary to optimize architectures and circuit topologies. Feature sizes continue to shrink, but as more functions are integrated on-chip the ratio of global routing distances to device dimensions is growing very large. Routing parasitics now dominate over intrinsic device parasitics, and at RF frequencies metallization is more accurately represented by transmission lines instead of lumped or distributed RC networks. To capture layout parasitics, hierarchical simulation of interconnect metallization is needed. Shown in Figure 3 is the UICchip, a 1.2-micron CMOS mixed-signal SOC developed at UIC. It includes a 50-MHz 8-bit microprocessor, 256-byte SRAM, a 400-MHz transceiver, and on-chip power management and regulation of three separate voltage supplies. Simulation of this SOC is challenging due to the interaction of digital and analog blocks which are operated at widely separated frequencies. An essential element in the accurate performance prediction of this project is extraction of device and interconnect parasitics. Logic is affected by increased switching times resulting in conservative estimates of cycle time. Without accurate estimation, analog and RF circuits may suffer from larger non-linearity and inaccurate biasing.

The UIC chip uses a full-custom logic implementation rather than synthesized gates to optimize performance of individual functional units. Silvaco has recently developed a suite of tools for this type of work. **Clever** is being applied to characterize the custom cells and ensure that critical timing margins are met. It is also being used to relate layout topography to specific RF performance metrics, to identify which layout geometries can optimize linearity and noise. To validate parasitic values extracted through simulation, fabricated test structures are required which characterize the resistance and capacitive coupling of multilevel interconnects. On-wafer measurements of these test structures will be compared with **Exact** simulations of identical structures. **Exact** can also be used to determine the range in interconnect parasitics due to process variations, essential in applying statistical process control to yield. Finally, at the chip-level, ***HIPEX*** extraction of all layout parasitics can be performed to compare the accuracy of hierarchical modeling with traditional flat lumped-element models. A significant feature of ***HIPEX*** is its interface to numerical simulation of complex regions.

Conclusions

In developing technologies and ICs for mixed-signal systems-on-a-chip, numerical simulation from the process to the IC layout parasitic extraction is needed to capture important second-order effects which critically impact reliability and performance. Digital systems cannot be approximated by simple switch-level simulations, and time- and frequency-domain simulation is required to analyze the fundamental analog nature of these circuits. For RF circuits, detailed device level simulation is necessary to optimize the internal structure for noise performance, linearity, and distortion. This type of optimization cannot be performed by assuming an equivalent circuit model. In designing for highest performance and lowest power, interconnect parasitics must be determined with a high degree of accuracy early in the design phase. The ***DISCOVERY*** tool suite is particularly well-suited for determining chip-scale device and interconnect parasitics. Its interfaces with numerical simulation of processes and devices are necessary in developing the on-chip matching networks that will emerge in SOCs operating at high frequency and low power.

References

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