Integrated Simulation Solution for Advanced Power Devices
Objectives of this Presentation

• Presentation of simulation results for non-silicon power device types
  • SiC Based Power Devices
  • GaN Based Power Devices
• IGBT Application examples:
  • IGBT Integrated Simulation Solution
  • Coupled optimization of diode and IGBT characteristics under clamped inductive switching in Atlas MixedMode and Virtual Wafer Fab (VWF)
• Doping challenges for SiC Technology:
  • Implantation is the only practical selective-area doping method because of extremely low impurity diffusivities in SiC
  • Due to directional complexity of 4H-SiC, 6H-SiC it is difficult to minimize or accurately predict channeling effects
  • Formation of deep box-like dopant profiles using multiple implant steps with different energies and doses
Measurement Verified Simulated Implant Profiles

Box profile obtained by multiple Al implantation into 6H-SiC at energies 180, 100 and 50 keV and doses 2.7 E15, 1.4E14 and 9E14 cm\(^{-2}\) respectively. Experimental profile is taken from T. Kimoto, A. Itoh, H. Matsunami, T. Nakata, and M. Watanabe, Journal of Electronic Materials 25, 879 (1996).
SiC Based Power Devices

Measurement Verified Simulated Implant Profiles

Aluminum implants in 6H-SiC at 30, 90, 195, 500 and 1000 keV with doses of 3x10^{13}, 7.9x10^{13}, 3.8x10^{14}, 3x10^{13} and 3x10^{13} ions cm^{-2} respectively. SIMS data is taken from S. Ahmed, C. J. Barbero, T. W. Sigmon, and J. W. Erickson, Journal of Applied Physics 77, 6194 (1995).
Channeling Dependant Phosphorous Implantation

Simulation of tilt angle dependence of Phosphorus ion implantation into 4H-SiC at 50 keV.
2D Monte Carlo Phosphorous Implantation into SiC

Multi-core computers significantly improve run times. This figure shows speedup achieved on 16 CPUs computer (Quad-Core AMD Opteron Processor 8356 x 4). The Well Proximity Effect was analyzed by running one million 300 keV Boron ion trajectories. 1 CPU: 6 h 40 min. vs 16 CPUs: 27 min.
Nitrogen Monte Carlo Implant into 4H-SiC Trench

- Tilted 20 degrees 25 keV Nitrogen implant into 4H-SiC trench
- Simulation time for one million trajectories took 5 minutes
The mobility behavior with SiC is anisotropic in nature. An anisotropic mobility model is implemented in Atlas to correctly model this behavior.
pn Diode Breakdown Voltage Simulation
- Extended precision simulation
GaN Based Power Devices

- Automated calculation of Spontaneous and Piezo-Electric Polarization
- Automated calculation of Strain for the whole InAlGaN material system
- X and Y Composition Dependent Models for Bandgap, Electron Affinity, Permittivity, Density of State Masses, Recombination, Impact Ionization, Heat capacity, Refractive Index, low and high field Mobilities
- GaN specific Impact Ionization and Field/Temperature Dependent Mobility Models
- Phonon-assisted tunneling model

Id vs. Vgs characteristics

Id vs. Vds characteristics.
After Optimizing Gate Field Plate Over-Lap, a 900 V breakdown voltage was obtained.
Self Heating Effects

- For GaN FETs on Sapphire or Silicon Carbide Substrates, Self Heating Effects are significant. This slide compares these effects on the resulting Id-Vg and gm Curves.
• Comparing IdVd Curves for a GaN FET on Sapphire and Silicon Carbide Substrates respectively
• IGBT Integrated Simulation Solution
  • We will present an IGBT design example comparing planar and trench type IGBTs using process and device simulation. The paper will complete the design flow by performing SPICE model parameter extraction and circuit simulation

• Coupled Optimization of Diode and IGBT Characteristics Under Clamped Inductive Switching in Atlas MixedMode and Virtual Wafer Fab (VWF)
  • VWF’s powerful range of optimizers are used to investigate and minimize the coupled switching losses of a TCAD IGBT and its clamping diode in a chopper circuit
In order to compare the performance of the planar and trench IGBT design, both should have a similar breakdown and threshold voltage.

- IGBT structure of Planar type (left) and Trench P N type (right)
Comparison of the Breakdown voltage

• Breakdown curve of Planar type (Red) and Trench type (Green)
• Same Breakdown Voltage
Comparison of the Threshold voltage

- Vge-Ic curves of Planar type (Red) and Trench type (Green) at Vce=10V
- Close Threshold Voltage
Comparison of the Saturation voltage

- Vce-Ic curves of Planar type (Red) and Trench type (Green) at Vgs=15V
- VCE(sat) at Ic=10A/mm²
  - Planar : 3.15V
  - Trench : 2.35V
Switching Circuit Schematic with Inductor Load

- Switching circuit of Inductor for Falltime measurement
- Gateway driven MixedMode simulation
- FWD (Free Wheel Diode) uses a Diode spice compact model
Comparison of Fall time

- Switching curves of Planar type (Red) and Trench type (Green) at 125°C
  - $T_f$: ②-① at $I_{CP} = 2.5\text{A/mm}^2$
    - Planar: 510ns
    - Trench: 470ns
Carrier Dependence on Switching Time (Trench)

- Distribution of Hole concentration during Switch-off

The tail current keeps flowing until the minority carrier (Hole) disappears
Performance comparison

- Tf vs VCE(sat) trade-off curves of Planar type (Red) and Trench type (Green) at different carrier lifetimes
• Owing to its surface-potential core, the bulk-MOSFET model HiSIM enables easy modeling extension to MOS-based power devices
• One of its derivatives is HiSIM_HV, the Compact Model Council standard model for high voltage (HV) MOS device
  • HiSIM_HV eliminates the traditional macro-modeling approach often used for power devices
• HiSIM-IGBT models the insulated gate bipolar transistor device by combining the advanced features of HiSIM, HiSIM_HV and a bipolar junction transistor model
An IGBT transistor is a combination of a MOS and a BJT transistor. In HiSIMIGBT, it is necessary to optimize the parameters of both devices simultaneously in order to obtain a suitable set of parameters. By using Utmost IV and the SmartSpice engine, optimization using the Genetic Algorithm becomes very practical. The solution enables fast and reliable parameter extraction.
ICBT Integrated Simulation Solution Spice Parameter Extraction

DC, and CV simulation results including temperature dependence
IGBT Integrated Simulation Solution Spice Parameter Extraction

Circuit Schematic

TCAD and SPICE simulation results
One of the fundamental goals when designing power devices is to minimize the energy losses in the circuit. These devices will be coupled with other standard circuit elements. Just because a stand-alone power device is optimized, this does not mean that when placed in a circuit the device parameters previously decided upon are still optimum in terms of energy loss.

In this presentation a MixedMode simulation of a chopper circuit will be performed and energy loss will be optimized using VWF.
The Atlas power devices (ADIODE and AIGBT) were combined in a chopper circuit which was created in MixedMode.
Coupled Optimization of Diode and IGBT Characteristics

Typical IGBT switching waveforms.
VWF is a tool that can be used for both Design Of Experiments (DOE) and Optimization Experiments. VWF can be used with Silvaco’s process, device, parameter extraction and circuit simulators.

To undertake an optimization experiment, one or more variables are chosen and VWF will then optimize these variables against a defined target.

The bulk lifetime in the IGBT and the bulk lifetime in the diode were chosen as variables in this example.

The turn-on, turn-off and on-state losses of the IGBT and diode were all monitored independently to see the effect had through varying the lifetimes not only on the system as a whole but on the individual components as well. The sum of the IGBT and diode switching losses was used as the optimization target.
Coupled Optimization of Diode and IGBT Characteristics

A section of the worksheet showing extracted values for the total energy loss for the circuit and for the individual IGBT and diode.

Graphical representation of the optimization experiment showing the total circuit energy loss versus iteration number.
Summary

• Silvaco delivers all key TCAD simulation solutions for all Power Device types in 2D and 3D

• The power device examples in this presentation illustrate Silvaco’s integrated TCAD and EDA design flow. Structural variations can be explored and designs can be optimized using process and device simulation. SPICE model parameters for HiSIM_HV and HiSIM-IGBT compact models can be extracted from TCAD-simulated data and used in SPICE circuit simulation. This enables the circuit designer to optimize the design before wafers are manufactured.