Simulation Standard

Connecting TCAD To Tapeout

A Journal for Process and Device Engineers

Temperature Dependence of Latch-up Holding Point for Majority Carrier Guards up to 250°C

D. Uffmann, J. Ackermann, J. Stemmer, J. Aderhold, and H.-U. Schröder
Laboratorium für Informationstechnologie, Universität Hannover
Schneiderberg 32, D-30167 Hannover, Germany

Introduction

Numerous applications would benefit from the availability of temperature resistant electronics. Among these are automotive electronic controllers for anti-blocking system, motor management and exhausting pipe gas analysis[1,2], aircraft electronics for engine control and replacement of hydraulic and pneumatic control[3] (e.g. More Electric Aircraft Initiative of U.S. Government). A further benefit is the reduction of cooling requirements for electronics. For the majority of these applications, mainly for those with economical importance, a maximum operating temperature of 250°C would be sufficient. For economical reasons the use of junction isolated CMOS devices, especially ASICs, is advantageous due to cost and short term availability.

A major drawback of junction isolated CMOS compared to SOI-CMOS is latch-up, which can be caused by leakage currents or dynamically by high signal edge slopes. Investigations show that the latch-up phenomenon implies increasing danger with rise of operating temperatures[4]. An improvement concerning latch-up resistance can generally be achieved by design precautions and technological measures. Considering a selected ASIC process we focus on design precautions.

CMOS ASIC Process

The investigations refer to a commercially available bulk twin tub LDD-CMOS ASIC process with epitaxial layer. Nominal gate lengths of the process are 1.0 micrometer, the effective gate lengths amount to 0.82µm and 1.0µm for the NMOS and PMOS transistor, respectively. The LOCOS process implies that the highly doped contact regions with junction depths of approximately 0.3µm exhibit oxide sidewalls. Tub doping is $2.8.10^{16}cm^{-3}$ with a junction depth of 3.8µm for the n-tub. The epitaxial layer has a total thickness of 13µm and is of p-type with doping of $1.0.10^{15}cm^{-3}$ on a highly doped p-substrate. The doping profiles were specified by the ASIC producer.

Latch-up Test Devices

Based on the analysis of mechanisms for latch-up triggering, we designed a set of latch-up test devices to examine different effects and parameters separately. Figure 1 shows a schematic cross section of the test devices. The surface topography of the test structures results from the fact that the interface between local oxide and silicon lies on the same plane as source and drain pn-junctions. Figure 1 also includes a lumped element circuit with parasitic bipolar transistors. In the n-tub two pnp-transistors are considered, a horizontal and a vertical device.

Test device 1 exhibits conventional electrode placement for reference. Type 2 devices serve to evaluate the effectiveness of majority carrier guard stripes. This refers to a device similar to type 1, where the positions of tub contacts and source regions are exchanged with each other. In type 2 configuration tub contacts are placed next to the inner p-tub-to-n-tub border. This configuration is not identical to majority carrier guard rings, which completely surround the emitters, but the mechanism of avoiding latch-up is basically the same. Majority carrier guards reduce sheet resistance of the tubs, fix the local potential and steer injected majority carrier currents away from the parasitic emitters. This results in a decoupling of the parasitic bipolars.[5] We have considered a device with the same geometry as

Continued on page 2.....

INSIDE

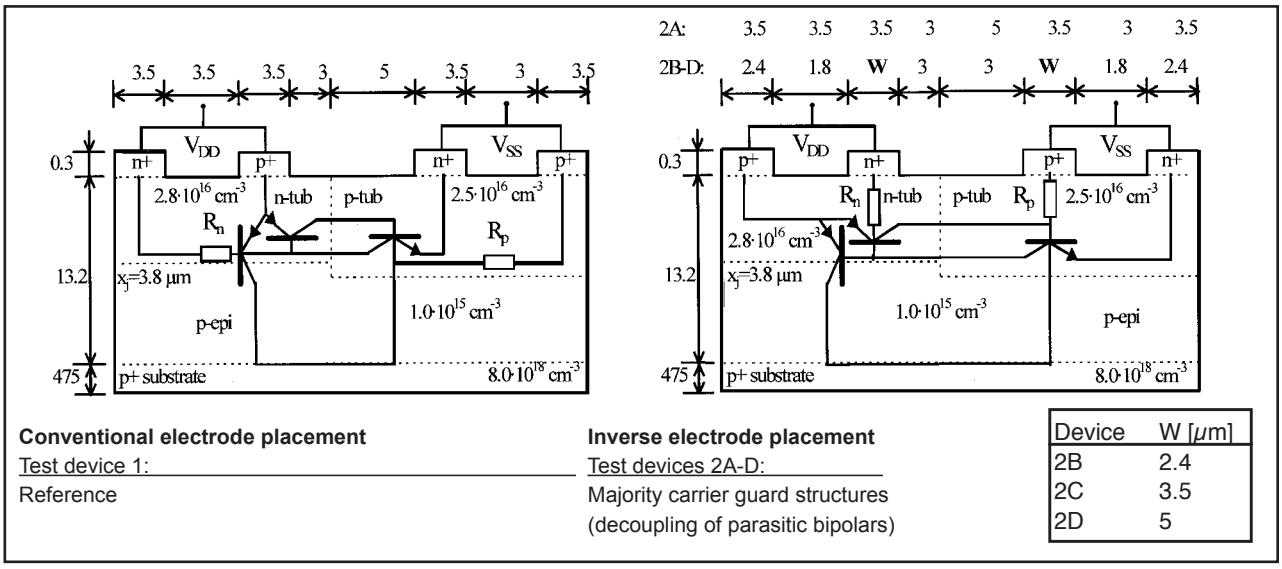

Figure 1. Schematic cross section of latch-up test devices with lumped element circuit.

device 1 that is referred to as 2A. Furthermore, 2B is a device with the minimum dimensions according to the design rules of the process and 2C has a slightly enlarged guard stripe width compared to 2B. We will also refer to an imaginary device 2D, that corresponds to 2B and C except that the width of the guard stripe is enlarged to 5µm. The width of all test structures is 25µm.

ATLAS Simulation of Latch-up Test Devices

Simulations were carried out using ATLAS/ SPISCES. Latch-up susceptibility has been evaluated in terms of holding voltage and holding current up to temperatures of 250°C. Our simulation procedure starts with a dynamical ignition of latch-up to get into the low-ohmic region of the test device. Afterwards the voltage is reduced until there is no convergence after reaching the holding point. We went through a careful selection procedure of physical parameter models. At the holding point the parasitic bipolar transistors are in saturation mode, meaning that all pn-junctions exhibit forward bias conditions.[13,10] The holding point is therefore characterized by high carrier injection levels and high carrier concentrations as well as degeneration effects. In order to get accurate results, we had to use appropriate models to describe these effects. We also used feedback from measurement results to corroborate simulation results. This led to the final selection, to consider the following models and effects:

- mobility µn,p(T) according to the model by Dorkel and Leturcq[6] including carrier-carrier scattering. This is very important with regard to the high injection levels at the holding point especially for the majority carrier guard structures.
- saturation velocity vsat(T)
- Auger recombination using temperature independent coefficients $c_n^{Auger}=2.8.10^{-31}cm^6/s$ and $c_p^{Auger}=9.9.10^{-32}$ cm^6/s after Dziewor [7] (there is only a small temperature dependence of Auger coefficients),
- Shockley-Read-Hall recombination: minority carrier lifetimes were extracted from leakage current measurements of process test devices, τ_p=138ns and τ_n=55ns; the temperature dependence was assumed to be $\tau_p \sim \sqrt{T}$ and $\tau_n \sim T^2$ according to Schmid and Reiner,[8]
- impact ionization after the model by Selberherr,[9]
- intrinsic carrier density $n_i(T)$,
- bandgap $E_g(T)$ with $E_g(300K)$=1.124eV after Selberherr[9], instead of the frequently used value for device simulation of 1.108eV,
- equivalent density of states $N_{C,V}(T)$.

The calculations were carried out using Fermi-Dirac-statistics instead of the commonly used Boltzmann-statistics. As a consequence we must not implement bandgap narrowing with its temperature dependence $\Delta Eg \sim 1/\sqrt{T}$.[10] Especially for high injection levels with carrier densities at the onset of degeneration in low doped regions Fermi-Dirac-statistics lead to considerably different results compared with Boltzmann-statistics in combination with bandgap narrowing.[11]

Results and Discussion

The measurements revealed typical latch-up characteristics of the test devices. The measured and simulated holding voltage of test device 1 is below 1.3V at room temperature. Sangiorgi et al.[12], Hu[13], and Wieder et al.[14] reported similar results for twin tub CMOS processes with epitaxial layer thickness of more than

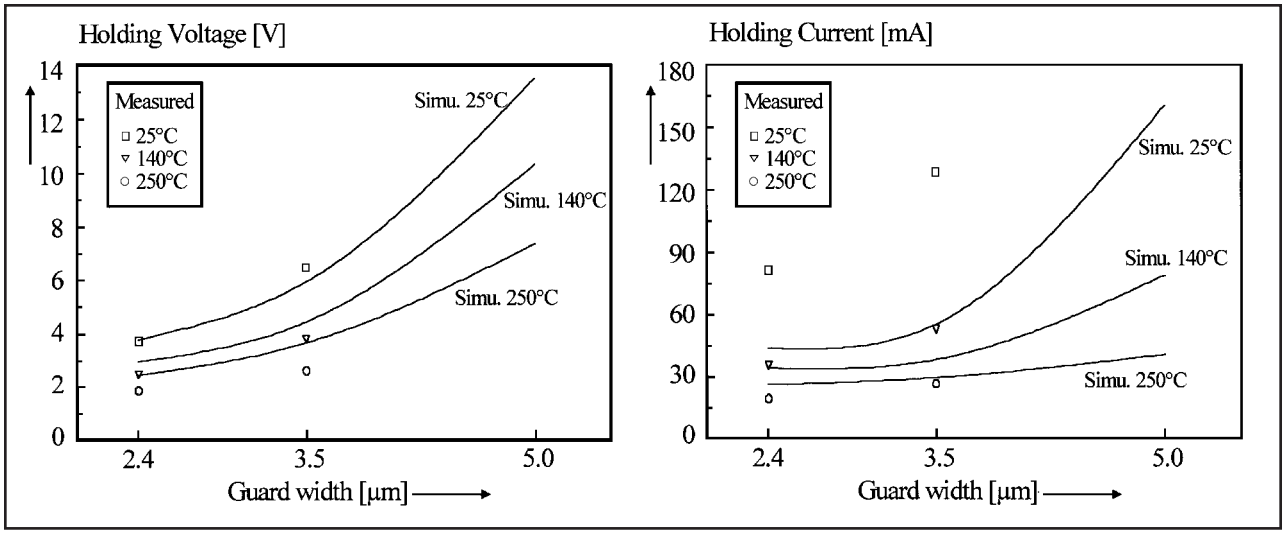

Figure 2. Measured and simulated holding voltage and current vs. width of guard stripes (2B-D).

7.5µm. The latch-up resistance of type 2 test devices is considerably higher than of type 1. At room temperature holding voltages of devices 2A and 2C are higher than 5V granting latch-up free operation for a supply voltage of 5V. Rung[15] has investigated a structure similar to type 2 at room temperature specifying a holding voltage of 5.5V. With increasing temperature the holding voltage and current decrease. At 250°C devices 2A, B and C exhibit holding voltages below 4V.

Simulation and measurement results for type 2 test devices match quite well at 140°C and 250°C, especially for the holding voltage. The holding current shows some mismatch, which is explained by self-heating and by the very high slope of the IV-curve near the holding point implying a higher inaccuracy for current values. At 250°C the measured holding voltages are somewhat lower than simulated values. This has to be kept in mind for the use of the simulator as a predicting tool. Nonetheless, in combination with the measurements, the results can be used to estimate the change of holding voltage for small changes of guard stripe width. This is performed using our imaginary test device 2D. An increase of the guard stripe width to W=5µm is sufficient to increase the holding voltage to a value higher than 5V at 250°C, even if accounting for the observed inaccuracy. Therefore, this design measure grants latch-up free operation. Figure 2 shows the influence of guard stripe width for devices 2B-D.

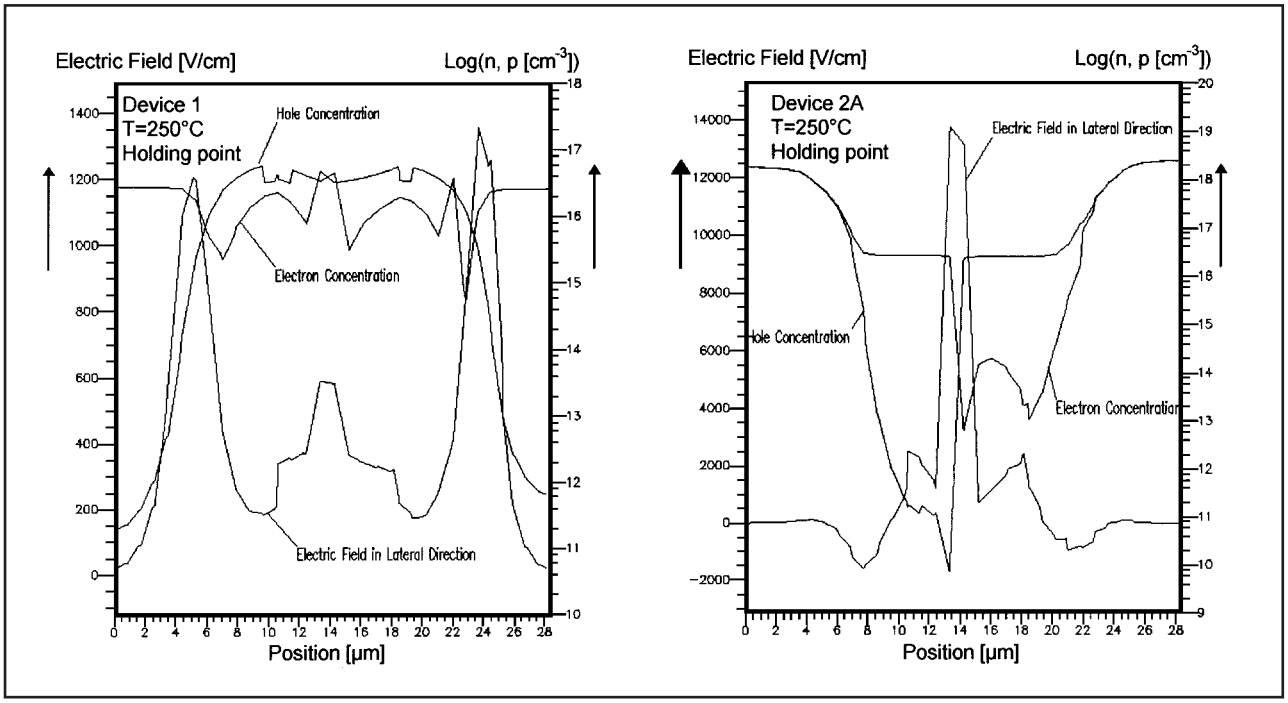

Figure 3. Electric field and carrier concentrations on a horizontal cutline (depth 1µm) at the holding point at T=250°C for device 1 (left hand side) and for device 2A (right hand side).

To explain the origin of the higher latch-up resistance of majority carrier guard structures up to high temperatures we discuss simulation results for the carrier densities and electric field in the devices 1 and 2A. These devices have the same distances and geometry except for the electrode placement. Figure 3 shows the carrier densities and electric field on a horizontal cutline in 1µm depth for a temperature of 250°C. Obviously, for device 1 the coupled bipolar transistors are in saturation mode with high carrier densities and low electric field at the tub border. A totally different behaviour is revealed for device 2A: the parasitic bipolars are in the active mode with high electric field and a space charge region of almost 2µm width at the tub borders. The region with high injection level is limited to the area beneath the parasitic emitters. This difference in the mode of operation of the parasitic bipolar transistors for conventional and inverse electrode placement is a new finding.

Conclusion

For majority carrier guard structures it is essential to use Fermi-Dirac-statistics instead of Boltzmann-statistics and a mobility model which accounts for carrier-carrier scattering in order to get accurate simulation results. The latch-up resistance of majority carrier guard structures (type 2) decreases with temperature as for conventional electrode placement (type 1). Nevertheless, for 5µm wide majority carrier guard stripes absolutely latch-up free operation up to 250°C is achieved.

References

1. J.L. Evans, C.S. Romanczuk, L.E. Bosley, and R.W. Johnson, “High temperature requirements for automotive electronic controllers”, Proc. 2nd Int. High Temp. Electron. Conf. (HiTEC), Charlotte, North Carolina, USA (1994), I-3-7.
2. J.C. Erskine, R.G. Carter, J.A. Hearn, H. L. Fields, and J.M. Himelick, “High temperature automotive electronics: trends and challenges”, Proc. 2nd Int. High Temp. Electron. Conf. (HiTEC), Charlotte, North Carolina, USA (1994), I-9-17.
3. M. Carlin and J. K. Ray, “The requirements for high temperature electronics in a future high speed civil transport”, Proc. 2nd Int. High Temp. Electron. Conf. (HiTEC), Charlotte, North Carolina, USA (1994), I-19-26.
4. K. Wu, and R.B. Brown, “High-temperature design rules”, Proc. 1st Int. High Temp. Electron. Conf. (HiTEC), Albuquerque, New Mexico, USA (1991), 267-272.
5. R.R. Troutman, Latchup in CMOS technology, Kluwer Academic Publishers, Boston (1986) 165-172.
6. J. Dorkel and P. Leturcq, “Carrier mobilities in silicon semi-empirically related to temperature, doping, and injection level”, Solid-State Electron. 24 (1981), 821-825.
7. J. Dziewor and W. Schmid, “Auger coefficients for highly doped and highly excited silicon”, Appl. Phys. Lett. 31 (1977) 346-348.
8. W. Schmid and J. Reiner, “Minority-carrier lifetime in gold-diffused silicon at high carrier concentrations”, J. Appl. Phys. 53, 9 (1982) 6250-6252.
9. S. Selberherr, Analysis and Simulation of Semiconductor Devices, Springer, Wien - New York (1984).
10. S.M. Sze, Physics of Semiconductor Devices, John Wiley & Sons, New York (1981), p. 143.
11. W. Engl and H. Dirks, “Models of physical parameters”, in Introduction to the numerical analysis of semiconductor devices and integrated circuits, Boole Press, Dublin (1981), 42-46.
12. E. Sangiorgi, R. L. Johnston, M. R. Pinto, P. F. Bechthold, and W. Fichtner, “Temperature dependence in scaled CMOS structures”, in IEEE Electron Dev. Lett., EDL1 (1986), 28-31.
13. G.J. Hu, “A better understanding of CMOS latch-up”, IEEE Trans. Electron Dev., ED-31(1) (1984), 62-67.
14. A. Wieder, C. Werner, and J. Harter, “Design model for bulk CMOS scaling enabling accurate latch-up prediction”, IEDM Tech. Dig. 1981, 354-358.
15. R.D. Rung and H. Momose, “DC holding and dynamic triggering characteristics of bulk CMOS latchup”, IEEE Trans. Electron Dev.,