

HiSIM



Analog/Mixed-Signal Simulation

Replacement of BSIM4 in UDSM Circuit Simulations

SILVACO

Analog / Mixed-Signal Simulation

Introduction

This paper presents HiSIM speed and convergence advantages against BSIM4 and PSP on a variety of circuits

- As technology dives under 90nm, it quickly becomes obvious that existing SPICE models such as BSIM3 and BSIM4 can not meet accuracy, simulation speed, convergence and model parameter extraction required by circuit designers
- HiSIM spice model was developed by Hiroshima University to meet stringent criterias of the UDSM world
- HiSIM is a physics based surface potential scalable compact model with easy to extract reasonable number of parameters. The robust physics enables HiSIM to meet all requirements for accurate transient, RF, noise and temperature circuit simulations

Analog / Mixed-Signal Simulation

Simulations – Compact Models Used for this Study

- BSIM3.3.0, BSIM4.5.0, PSP-102.1 (Oct. 2006 release) and HiSIM-2.3.1 (Nov. 2006) were used in this study
- All model parameters except BSIM4 were extracted using Compact Model Council (CMC) undisclosed measurement data under the chairman's permission. BSIM4 model parameters were provided for CMC member evaluations

Analog / Mixed-Signal Simulation

Simulations – Circuits used for Simulations/Test Environment

- Commercial circuits addressing the size and complexity of circuits are selected from various customers. Circuits are known to be good and in production of 90 nm technology
- Silvaco SmartSpice 64bit, version 3.3.0B was used. The computer used was Sun Micro Systems ULTRA 40 (AMD Opteron 2.4 GHz (4 CPUs), 8 Gbytes main memory, swap 10 Gbytes) running Red Hat Linux Enterprise WS3. All jobs were run on 1 CPU under batch silent mode

Analog / Mixed-Signal Simulation

Simulation Results

	BSIM3	BSIM4	HiSIM	PSP
Circuit -1:	5275	15,495	18,745	Failed
Circuit -2:	1048	3958	2895	Failed
Circuit -3:	120	414	333	752
	(223)	(739)	(523)	(3448&Stop)
Circuit -4:	11m13	28m55	26m05	53m16
Circuit -5:	19	157	139	274
Circuit -6:	9m52	63m02	27m44	Failed
Circuit -7:	149m25	21h9m	97m14	21h9m
		(MC#308)		(MC#396)
Circuit -8:	612m33	1935m31	407m58	Failed
				(after 53m34)

(Simulation time in seconds)

Analog / Mixed-Signal Simulation

Simulation Results (con't)

- Circuit -1
 - 10 bit ADC @24Mhz (Image sensor application)
 - Devices : 4483, Vsources : 9, Caps : 258, Res : 28, Vdd: 1.2V
- Circuit -2
 - Active Driver, part of LD, full chip and DC-DC converter
 - Devices : 393, Vsources : 7, 9, Caps : 7, Res : 29, Vdd : 1.2 V
- Circuit -3
 - Fractional PLL
 - Devices: 8,771, Vsource: 48, caps : 9 , Res : 55, Vdd : 1.1 V
- Circuit -4
 - I/O Module,
 - Devices: 18,888, Vsource: 182, caps : 35,646 , Res : 304, Vdd : 1.1 V

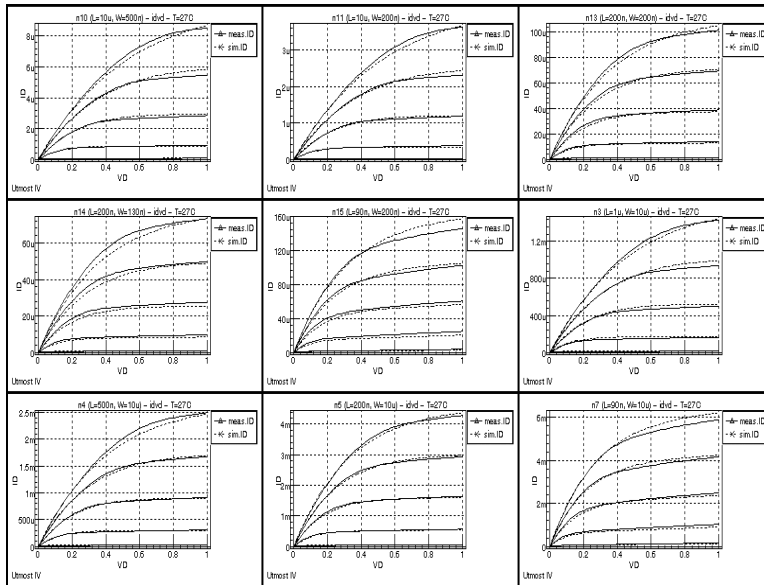
Analog / Mixed-Signal Simulation

Simulation Results (con't)

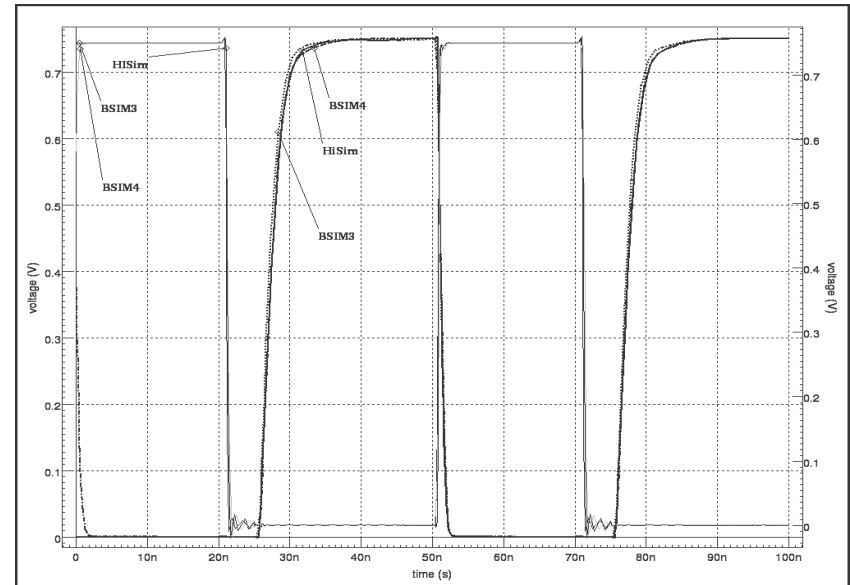
- Circuit -5
 - VCO
 - Devices : 55, Vsouces: 6, Caps: 96, Res: 0, Vdd: 1.2
- Circuit-6
 - DLL (Delay Lock Loop)
 - Devices: 5941, Vsources : 104, Caps: 50, Res: 13, Vdd: 1.2 V
- Circuit -7
 - 32-bit Parity Checker
 - Devices: 1727, Vsources: 70, Caps: 66, Res: 53, Vdd: 1.2 V
- Circuit – 8
 - Mux Buffer
 - Devices: 196496, Vsources: 59, Caps: 402464, Res: 411428, Vdd: 1.1 V

Analog/Mixed-Signal Simulation

Example of HiSIM Model Extraction Accuracy/Circuit Simulation Accuracy



Example of Scalable 90nm HiSIM Model



HiSIM Simulation shows good accuracy

Analog / Mixed-Signal Simulation

Acknowledgement/References

- The authors would like to thank CMC chairman Dr. Josef Watts for the use of CMC data for this study
- Compact Modeling Council home page
<http://www.eigroup.org/CMC/default.htm>