Electrical Stress Degradation of Small-Grain Polysilicon Thin-Film Transistors

Domenico Palumbo, Silvia Masala, Paolo Tassini, Alfredo Rubino, and Dario della Sala


Abstract—This paper is focused on the stability of n-channel laser-crystallized polysilicon thin-film transistors (TFTs) submitted to a hydrogenation process during the fabrication and with small grains dimension. With the aid of numerical simulations, we investigate the effects of static stress using two types of procedures: the on stress and the hot carrier stress. Results show that the variations of trap state density into the whole polysilicon layer and not only near the drain junction are responsible for the degradation of TFTs performances in both the two types of stress and that the interface trap states play a negligible role compared to the bulk trap states.

Index Terms—Density-of-states (DoS), fixed charge, numerical simulation, reliability, thin-film transistor (TFTs).

I. Introduction

LASER-CRYSTALLIZED polycrystalline silicon thin-film transistors (TFTs), processed at a low temperature (below 600 °C), are devices of great importance in the microelectronics industry since they are currently widely used in active-matrix liquid crystal displays and are suitable for the emerging activematrix organic light emitting displays (AMOLED) [1].

By using low laser energy densities up to 200 mJ/cm², we have fabricated devices with small grains dimension with a mobility of up to about 3 cm²/V·s. These n-TFTs are suitable not only to drive an OLED diode [1], [2] but also to realize the row drivers [3]; moreover, the increased uniformity of electrical parameters, compared to large grains size TFTs, gives rise to a reduction, for instance, of the threshold voltage spreading [4], avoiding more complicated pixel circuit to overcome this problem [5], [6] and obtaining brightness uniformity over large areas.

Their drawback is the instability after electrical stress [7], [8], due to a high density of in-grain and grain boundary defects, to poor properties of the gate insulator and to poor polysilicon/oxide interface [9].

The purpose of this paper is to understand which are the main mechanisms originating from device degradation under a bias stress. This is accomplished by comparing the computer simulation of device characteristics with the experimental data.

II. Fabrication Details

Polysilicon TFTs were fabricated on 1737 Corning glass substrate by low temperature processes. An amorphous silicon film, 100-nm thick, was deposited by plasma enhanced chemical vapor deposition (PECVD) at 200 °C and 0.75 torr using pure SiH₄ (20 sccm).

The source and drain regions were obtained by the PECVD deposition of an n-type layer, 23-nm thick (λ = 120 °C, p = 0.75 torr, with a SiH₄/P₂H₅ = 98/2 gas ratio, and 20 sccm). For the patterning of the drain and source electrode areas, the lift-off method were used, with silicon oxide as the sacrificial layer. The a-Si:H, the sacrificial oxide, and the resist layers are deposited in sequence; after resist development and curing, the sacrificial layer is etched by a buffered HF (a solution of HF and NH₄F). This step determines, for the subsequently deposited n layer, a discontinuity which helps the resist lift off performed by acetone. In this way, the undesired n layer is removed as well. Next, the buffered HF bath completely removes the sacrificial oxide.

The dehydrogenation before laser crystallization was performed, keeping the material for 8 h in vacuum at 450°C.

After the PECVD growth, the doped and undoped amorphous films were crystallized by XeCl excimer laser irradiation at λ = 308 nm, with a 130 x 13 mm beam diameter and with a 200-mJ/cm² energy density on the sample.

The active regions of TFTs were patterned by CF₄ plasma etching (CF₄ 40 sccm, 0.35 torr, and rf power = 15 W). Then, a hydrogen plasma passivation was performed on...
the polysilicon layer for 30 min at 400°C ($p = 0.99$ torr and rf power = 6 W) to reduce the defect density inside the film and to improve the electrical characteristics of TFTs. The gate oxide, 100-nm thick, was deposited at 300°C and 0.40 torr by PECVD. Finally, the drain and source contact opening by wet etching (buffered HF), metal evaporation, and contact definition were performed to complete the structure (see Fig. 1). TFTs are produced through a four-mask process using the AZ5214E photo resist.

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### III. Characterization Before Electrical Stressing

The output and transfer characteristics before electrical stressing were measured at room temperature using a semiconductor parameter analyzer HP4140B. First, the output characteristics were measured at five different gate biases (0.1, 4.1, 8.1, 12.1, and 16.1 V), varying the drain voltage between 0 and 30 V; then, the transfer characteristics were measured at five different drain biases (0.1, 5.1, 10.1, 15.1, and 20.1 V), varying the gate voltage between −13 and 30 V (see Fig. 2).

Fundamental parameters were extracted by extrapolation of the curve $I_{DS} = V_{DS}$ and in particular, in the linear regime, e.g., for $V_{DS} = 0.1$ V, $V_{DS} - V_T$, the approximate expression for $I_D$ reduces to

$$I_{DS} = \frac{W}{L} \mu_n C_i [(V_{GS} - V_T) V_{DS}]$$  \hspace{1cm} (1)

so that the threshold voltage $V_T$ is the voltage at which the aforementioned linear fit of $I_{DS}$ is zero; its average value is $7.8 \pm 3\%$, for a deposition area of about 1.5 × 2 cm. The electron mobility extracted by (1) is about 3 cm²/V·s ± 4%, and this value agrees with the correlation between the carrier mobility and the grain size proposed by Wagner et al. [10]; the inverse subthreshold slope $S$ was determined from the inverse slope of the $I_{DS} - V_{DS}$ characteristic in the subthreshold region ($V_{GS} < V_T$), that is the linear region of the semilogarithmic transfer characteristics

$$S = \frac{\partial V_{GS}}{\partial \log I_{DS}}.$$  \hspace{1cm} (2)

### IV. 2-D Numerical Simulation of I–V Characteristics Before Electrical Stressing

In order to analyze the electrical characteristics of polysilicon TFTs, we performed 2-D numerical simulations using the commercial device simulator Silvaco-ATLAS [11].

The simulation grid comprises 1700 nodes, and it is heavily refined in the channel region (here, the distance between two nodes is less than 10 nm).

![Fig. 1. Cross section of polysilicon TFT used in this paper.](image1)

![Fig. 2. Characterization of n-channel TFTs (W = 40 µm and L = 5 µm). (a) Transfer characteristics at different gate voltages VGS. (b) Output characteristics at different drain voltages VDS.](image2)
The fine grain structure of our polysilicon produces a large in-grain defect density; this is why our analysis is based on a continuous trap model, and we have simulated a spatially uniform density-of-states (DoS), throughout the volume of the polysilicon layer. Our film can be considered as composed of small crystalline grains embedded in an amorphous tissue: the grain boundaries have a dimension comparable with the grain, so its properties, (Eg) and DoS, influence electron transport mechanisms, limiting, for instance, the mobility value and determining the overall electrical characteristics [12]. We have modeled the grain boundaries as a-Si:H.

It is worthwhile to point out that numerical simulation using a gap value of 1.12 eV does not fit the experimental results. Instead, the best results are obtained with Eg = 1.6 eV [13], [14].

The total DoS g(E) was modeled by the sum of two exponential tails near the conduction and the valence and two deep level bands with Gaussian distribution (one acceptorlike and the other donorlike). The model was [11]

\[
g(E) = \text{NTA} \exp \left( \frac{E - E_C}{\text{WTA}} \right) + \text{NTD} \exp \left( \frac{E - E_T}{\text{WTD}} \right) + \text{NGA} \exp \left( \frac{E - \text{EGA}}{\text{WGA}} \right)^2 \right) + \text{NGD} \exp \left( \frac{E - \text{EGD}}{\text{WGD}} \right)^2 \right) \right] \right).
\]

The initial parameters of the upper-half gap DoS were obtained from experimental I–V curves using the method by Suzuki et al. [15], [16], so that the interface states density has been considered negligible compared with the bulk states density. This assumption has been confirmed by simulation.

The electron and hole mobilities were modeled as constant throughout the channel and independent of: 1) the transversal electric field; 2) the gradient of the quasi-Fermi potentials; and 3) the doping level. The doping distribution was kept uniform throughout the polysilicon layer.

Table I summarizes the material parameters that provides the best accordance with the experimental curves of realized devices, while the consequent DoS parameters are: \( \text{NTA} = 9.2 \times 10^{20} \text{ cm}^{-3} \cdot \text{eV}^{-1} \), \( \text{NTD} = 2.0 \times 10^{12} \text{ cm}^{-3} \cdot \text{eV}^{-1} \), \( \text{NTA} = 0.1 \text{ eV} \), \( \text{WTA} = 0.1 \text{ eV} \), \( \text{WTD} = 0.1 \text{ eV} \), \( \text{NGA} = 5.0 \times 10^{12} \text{ cm}^{-3} \cdot \text{eV}^{-1} \), \( \text{NGD} = 1.0 \times 10^{10} \text{ cm}^{-3} \cdot \text{eV}^{-1} \), \( \text{EGA} = 0.6 \text{ eV} \), \( \text{EGD} = 1.0 \text{ eV} \), \( \text{WGA} = 0.4 \text{ eV} \), and \( \text{WGD} = 0.4 \text{ eV} \).

An important issue is that, to simulate the transfer characteristics, we have to increase the density of the positive fixed charge (\( Q_f \)) at the interface between polysilicon and SiO\(_2\), from \( Q_f = 0.95 \times 10^{12} \text{ cm}^{-2} \) for \( V_{DS} = 0.1 \text{ V} \) to \( 1.40 \times 10^{12} \text{ cm}^{-2} \) for \( V_{DS} = 20.1 \text{ V} \), as shown in Fig. 3. The increase of the positive fixed charge combined with a constant density of deep states reproduces the progressive shift of the subthreshold region observed during the characterizations, as a result from the good agreement between

<table>
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<th>Parameters</th>
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<td>( m_n )</td>
<td>Electrons mobility</td>
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<td>cm(^2)/Vs</td>
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<td>( m_p )</td>
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<tr>
<td>( n_{300} )</td>
<td>Conduction band density of states at 300K</td>
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<td>cm(^{-3})</td>
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<td>( e_{300} )</td>
<td>Energy gap at 300K</td>
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<td>eV</td>
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<td>( \tau_{p0} )</td>
<td>Shockley-Read-Hall lifetime for holes</td>
<td>1 \times 10^6</td>
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Table 1. Parameters used in the numerical simulation.
the experimental and simulated data shown in Fig. 4. Actually, during the characterization, we dynamically stress the devices, so we may suppose that these positive and negative bias stresses cause charge trapping in the gate oxide and alter the “fixed-charge” at the interface between the oxide and semiconductor, producing a translation without any slope variation of the measured characteristics. Specifically, negative bias stress leads to positive charge trapping, which means an increase in the positive fixed charge density; similarly, positive bias stress reduces the positive fixed charge density, as explained by Powell et al. [17]. The resulting total density of the fixed charge depends on the global dynamic stress, and in our case, the positive fixed charge increases with linear dependence on the stressing time. Instead, by changing the DoS in the bulk of the film (varying the values of DoS parameters listed in this section) or the interface defect traps at discrete levels within the bandgap of the semiconductor (with the Atlas INTTRAP parameter), the simulation failed to reproduce the shift of the subthreshold region observed in the experiments.

V. Static Bias Stress

In order to analyze the degradation of polysilicon TFTs caused by static electrical stress during, for example, the OLED driving in the AMOLED displays, we have used two types of conditions: the “on stress,” with \( V_{GSO} = 20 \) V and \( V_{GSO} = 0 \) V [12], and the “hot carrier stress,” with \( V_{GSO} = 20 \) V and \( V_{DS} = 25 \) V [18], [19], as a function of the stressing times. The first one is used to study the effects of electron accumulation during a positive stress and the effects of carriers flowing in to the gate oxide; the second one is used to study the degradation arising from impact ionization in the high electric field region close to the drain junction. Different devices, showing similar starting electrical characteristics and “dynamic stress effect,” have been used for each type of stress; the output and the transfer characteristics were recorded at 100, 1000, 2000, and 10 000 s, and the stress effect on the threshold voltage and on the subthreshold slope variation was calculated as \( \Delta V_{S} = V_{S}^{20} - V_{S}^{0} \) and \( \Delta S = S_{i} - S_{r} \) respectively, from the transfer characteristics measured at \( V_{GSO} = 0.1 \) V. \( V_{S}^{20} \) and \( S_{i} \) represent the initial values of \( V_{S} \) and \( S \), while \( V_{S}^{0} \) and \( S_{r} \) represent, respectively, the values of \( V_{S} \) and \( S \) at each stress time.

Fig. 5 shows the quantitative changes of \( S \) and \( V_{S} \) extracted from the stressed transfer characteristics measured at \( V_{GSO} = 0.1 \) V as a function of the stressing time.

With a pure \( V_{GSO} \) stress, carrier-induced gap states creation into the polysilicon has been proposed as the dominant mechanism to explain \( V_{S} \) shift toward more positive values [20]; actually, the threshold voltage, for polysilicon TFT [21] in which the effect of grain boundary trap density dominates, can be written as [22]–[24]

\[
V_{T} = \phi_{MS} - \frac{Q_{f}}{C_{ox}} + 2 \frac{kT}{q} \ln \left( \frac{n}{N} \right) + \frac{4 \epsilon_{si} N k T \ln \left( \frac{N}{n} \right)}{C_{ox}}
\]

where \( \phi_{MS} \) is the workfunction difference between the gate and polysilicon channel, \( Q_{f} \) is the fixed oxide charge density, \( C_{ox} \) is the oxide capacitance per unit area, \( N \) is the trap density, \( n \) is the intrinsic carrier concentration, \( \epsilon_{si} \) is the dielectric permittivity of SiO\(_{2} \), \( q \) is the electron charge, \( k \) is the Boltzmann’s constant, and \( T \) is the absolute temperature.

Concerning the inverse subthreshold slope \( S \), if we assume that the density of the deep bulk states and the interface states are independent of the energy, it is directly related to the DoS by the following relation [25]–[27]:

\[
S = \frac{kT}{q} \left[ 1 + \frac{C_{D} + C_{ts}}{C_{ox}} \right] \ln 10
\]
where $C_D$ is the depletion layer capacitance per unit area and $C_p = q D_p$ with $D_p$ (per square centimeter electronvolt) as the density of the total trap states. For fully depleted TFTs with thin and intrinsic channel (in other words if the band bending occurs in the whole polysilicon layer), we have

$$D_{ts} = D_{\text{bulk}} t_{si} + D_{it}$$

(6)

where $D_{\text{bulk}}$ (per cubic centimeter electronvolt) is the mean bulk trap density, $D_{it}$ (per square centimeter electronvolt) is the interface trap density, and $t_{si}$ is the polysilicon film thickness.

Following the method of Rolland et al. [27] we have determined the upper values of $D_{\text{bulk}}$ and $D_{it}$ for our TFTs

$$D_{it} = 10^{13} \text{ cm}^{-2}\text{eV}^{-1} \quad D_{\text{bulk}} = 1.7 \times 10^{10} \text{ cm}^{-3}\text{eV}^{-1}.$$  

(7)

Although this method is not very precise, it permits a coarse estimation of relative trap density. In our TFTs, about 95% of $D_{ts}$ is due to the bulk states, and only 5% of $D_{ts}$ is due to the interface states.

Under “on stress” conditions, both $S$ and $V_T$ show a logarithmic dependence on the stressing time (see Fig. 5): this behavior is consistent with a mechanism of stress-induced creation of acceptorlike traps, negatively charged when occupied by electrons [12], and means that the observed degradation effects are not caused by electron effects or charge injection into the gate dielectric, but they arise from the variation of bulk states density [28].

The degradation effects on the transfer characteristics after 100, 1000, and 10 000 s of hot carrier stress are similar to those presented after positive gate bias stress conditions (see Fig. 5), also with the source and drain reversed. The application of an additional drain stressing bias to the gate stressing does not have a relevant effect on the
degradation of the TFT parameters, despite the higher field between the source and drain. Therefore, we can suppose that our devices are more sensitive to gate stress than to drain stress because they present small polysilicon grains size [29] and that, on the contrary to what is suggested by some authors [30], [31], we do not have a damaged region near the drain contact.

VI. 2D Numerical Simulations of Stressed TFTs

The stressed transfer characteristics are simulated using the mesh used previously in the unstressed devices, the parameters presented in Table I, and a constant positive fixed charge ($Q_f = 1.40 \times 10^2 \text{ cm}^{-2}$) at the interface between the oxide and semiconductor.

Simulation performed with the interface defect traps at the discrete energy levels within the bandgap of the semiconductor failed to reproduce the experimental characteristics, similar to what has been deduced by Hatzopoulos et al. from his stress experiments [30]. This confirms the considerations in Section V. Actually, since hydrogenated poly-Si TFTs with a large ratio between the channel length and grains size have a large amount of Si–H bonds inside the film rather than at the interface with the gate oxide [32], the characteristics of TFTs are mainly determined by the defects in the bulk of the polycrystalline silicon film.

Both the transfer characteristics measured after different time of “on stress” and “hot carrier stress” states are reproduced in the numerical simulation, considering the DoS parameters listed in Section IV, with only one variation: the density of the tail states at the conduction band (NTA), as shown in Fig. 6. Fig. 7 shows an example of the simulated transfer characteristics.

In accordance with Wu et al. [29] and due to the dimensions of the polysilicon grains size, the degradation rate of our devices seems to depend only on the gate bias, and it is independent of the drain bias, as shown in Fig. 5.

In general, it is difficult to envisage a unique degradation mechanism that explains the variation of $S$ and $V_T$, because it may depend on the hot carrier injection in the gate oxide or/and on the creation of trap states at grain boundaries and/or at the interface between the oxide and polysilicon [26]. From the simulation results, we can say that the main degradation mechanism is the generation of defects in the gap of polysilicon mainly in the upper half of the bandgap.

The tail states are located in the structurally disordered silicon regions with strained bonds [33] and are easily broken [34], so they are likely to break under electron accumulation and they create shallow acceptor tail states in the upper part of the bandgap in the case of n-type TFTs [35].

We therefore suggest, according to the 2-D simulations, that in our devices, as a consequence of the breaking of the Si–H bonds, a hole trapping occurs in the polysilicon film that creates acceptor-type states, that are neutral when empty and negatively charged when filled and whose occupation is determined by the Fermi level.

VII. Conclusion

Stress mechanisms on low-temperature polysilicon TFTs have been investigated, both experimentally and theoretically, by means of numerical simulations. Two significant results were obtained. The measurement of $I_{ds}^{-V_{ds}}$ and $I_{ds}^{-V_{gs}}$ characteristics determines a dynamic stress of TFTs and the increase of positive fixed charge without any variation of defect density neither at the interface nor into the polycrystalline silicon film. On the other hand, static bias stress determines an increment of the acceptor tail states defects within the entire layer of polycrystalline silicon film, without any change in the fixed charge density. These considerations are supported by the 2-D numerical simulation. Furthermore, the stress mechanisms are not related to the variation of the interface states because of a high ratio between the channel length and grain size and there is no region near the drain electrode, which is damaged because of the hot carrier stress.

References


