Berkeley Common-Gate Multi-Gate MOSFET Model
• When we reach the end of the technology roadmap for the classical CMOS, multi-gate (MG) CMOS structures will likely take up the baton. Numerous efforts are underway to enable large scale manufacturing of MG FETs. At the same time, circuit designers are beginning to design and evaluate multi-gate CMOS circuits.

• A BSIM-CMG compact model is developed at Berkeley University in order to meet the present and future needs of circuit developers (short term) and circuit designers (long term) using MG nano-FET technology.

• BSIM-CMG model provides maximum **versatility** (regarding multi-gate device geometry and technology) without compromising **ease of use** and computational **efficiency**.

• BSIM-CMG has been developed to model the electrical characteristics of Common MG (CMG) structures (all gates are electrically tied together). A separate model, the BSIM-IMG, has been developed to model the Independent MG (IMG) structure, but it is not yet officially released.
Versatility of Multi-Gate FET Structures in BSIM-CMG

Users can specify the MG structure of interest via the geometry mode selector (GEOMOD)

- **Double Gate**
  - GEOMOD=0
  - Materials: Silicon, Gate, SOI

- **Triple Gate**
  - GEOMOD=1
  - Materials: Silicon, Gate, SOI

- **Quadruple Gate**
  - GEOMOD=2
  - Materials: Silicon, Gate, SOI

- **Cylindrical Gate**
  - GEOMOD=3

BSIM-CMG is implemented in two versions (modes of operation): three-terminal BSIMCMG-SOI mode (with D, G, S ports) and 4-terminal BSIMCMG-BULK mode (with D, G, S, B ports).
• Physical surface-potential-based formulations are derived for both intrinsic and extrinsic models with finite body doping
• The surface potentials at the source and drain ends are solved analytically with poly-depletion and quantum mechanical effects. If the channel doping concentration is low enough to be neglected computational efficiency can be further improved by setting COREMOD = 1
• The effect of the finite body doping is captured through a perturbation approach.
• The analytic surface potential solution agrees with 3-D device simulation results without fitting parameters
Treatment of the Corner Effects

- The corner transistor needs to be modeled separately
- First order model is a quarter-cylindrical MOSFET
- Developed also a quarter-cylinder model including finite doping

Electron concentration in different MG structures operating in saturation (Silvaco Atlas-Device 3D)
• Volume inversion is included in the solution of the Poisson’s equation
• Analysis of the electrostatic potential in the body of MG MOSFETs provided the model equation for the short channel effects (SCE). The extra electrostatic control from the end-gates (top/bottom gates) (triple or quadruple-gate) is also captured in the short channel model
• Hybrid-surface-orientation mobility, corner-induced effective width reduction, and end-channel-enhanced electrostatic control are modeled for different MG structures for efficient computation
• BSIM-CMG provides the flexibility to model devices with novel materials. This includes parameters for non-silicon channel devices and High-K/Metal-gate stack
• Other important effects, such as, mobility degradation, velocity saturation, velocity overshoot, series resistance, channel length modulation, quantum mechanical effects, gate tunneling current, gate-induced-drain-leakage, temperature effects, thermal/flicker/shot noise, and parasitic capacitance, are also incorporated in the model
Model Verification: Symmetry at Vds=0

![Diagram showing the normalized capacitance and the derivative of the drain current with respect to the drain voltage](image)

- **Symbols**: TCAD
- **Lines**: Model

**Normalized Capacitance**
- Cgg
- Cgs
- Csg
- Cdg
- Cgd

**Drain Voltage (V)**
- Na = 3e18 cm⁻³
- Vgs = 1.5 V

**Derivative**: \( \frac{d^3I_{ds}}{dV_x^2} (A/V) \)

**Graph**: 
- \( V_g = 0.0 \)
- \( V_g = 0.2 \)
- \( V_g = 0.4 \)
- \( V_g = 0.6 \)
- \( V_g = 0.8 \)
- \( V_g = 1.0 \)
Model Verification: Global Fitting for nFETs

Vds=50mV

Drain Current (A) vs. Gate Voltage (V)

Transconductance (A/V) vs. Gate Voltage (V)

Drain Voltage (V)

Lg = 90n

Vgs=1.0V

Vgs=0.8V

Vgs=0.6V

Vgs=0.4V

Drain Current (A)

Gate Voltage (V)

Output Resistance (Ω)

Drain Voltage (V)

Berkeley Common-Gate Multi-Gate MOSFET Model

- 8 -
BSIM-CMG v103.0 in SmartSpice

17 Stage Ring Oscillator Berkeley Test Example

![Graph showing voltage over time for 17 Stage Ring Oscillator Berkeley Test Example]
## Berkeley BSIM-CMG Release History

<table>
<thead>
<tr>
<th>Date</th>
<th>Release Version</th>
<th>Modifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>2006.10.2</td>
<td>BSIM-CMG 1.0-alpha</td>
<td>Basic core I-V, C-V model, short channel effects, field dependent mobility/velocity saturation, GIDL, gate tunneling current, quantum Effects</td>
</tr>
<tr>
<td>2007.8.26</td>
<td>BSIM-CMG 1.0</td>
<td>Binning equations, output conductance, $I_{gs}$, $I_{gd}$</td>
</tr>
<tr>
<td>2008.1.10</td>
<td>BSIM-CMG 1.0.1</td>
<td>Bug fixes</td>
</tr>
<tr>
<td>2008.11.8</td>
<td>BSIM-CMG 1.1.0-alpha</td>
<td>External $R_{ds}$, Temperature effects, Flicker/thermal/shot noise models, NQS gate resistance,</td>
</tr>
<tr>
<td>2009.5.10</td>
<td>BSIM-CMG 102.0 (also official release of 1.1.0)</td>
<td>Parasitic Resistance/Capacitance Models, Gmin.</td>
</tr>
</tbody>
</table>
Berkeley Release History

<table>
<thead>
<tr>
<th>Date</th>
<th>Release Version</th>
<th>Modifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>2009.10.1</td>
<td>BSIM-CMG 103.0</td>
<td>Cylindrical gate geometry with an associated short channel scale length and quantum effects model. Polydepletion model. Self-heating with addition of a temperature node. Asymmetry in GIDL/GISL currents. Junction capacitance and junction current equations with source-drain asymmetry. Introduction of SHMOD, RGATEMOD, NQSMOD and RDSMOD flags to control the number of internal nodes for faster simulations.</td>
</tr>
</tbody>
</table>