PDK-Based Analog/Mixed-Signal/RF Design Flow
Silvaco Analog/Mixed-Signal/RF PDKs

- What is a PDK?
- Which people build, use, and support PDKs?
- How do analog/mixed-signal/RF engineers use a PDK to design ICs?
- What is an analog/mixed-signal/RF design flow?
- How do you build a good PDK?
- How do you measure quality of PDK?
  - What is the FSA PDK Checklist?
  - How do you support designers using a PDK?
What is a PDK?

- A process design kit (PDK) is a collection of verified data files that are used by a set of custom IC design EDA tools to provide a complete analog/mixed-signal/RF design flow.
- These data files include schematic symbols, SPICE models, Parameterized Cells (PCELLS), DRC/LVS runsets, parasitic extraction runsets, and scripts that run by the EDA tools to automate the generation and verification of design data.
Who are the People Who Build and Use PDKs?

- Foundries Manufacture Silicon Wafers
  - Build PDKs for their customers
- Electronic Design Automation Vendors Make Software Tools
  - Build PDKs for their customers
- Fabless Semiconductor Companies Make Integrated Circuits
  - Use PDKs to Design ICs
- Integrated Device Manufactures (IDM)
  - Manufacture and Design ICs, build and use PDKs
- ASIC Vendors
  - Design ICs for System Designers, build and use PDKs
- System Designers
  - Manufacture Cell Phones and other products
Why Adopt PDK Design Methodology?

• Jump-starts designers with an instantly productive environment for new design projects – DESIGN PRODUCTIVITY

• Ensure manufacturing success with pre-configured schematic symbols and layout technology files – DESIGN QUALITY

• Tightly links EDA tools, IC designers, and foundry support for fast time-to-market – TAT

• Reduces costly rework cycles – PROFITABILITY

*Rapidly becoming industry standard for analog circuit design methodology*
PDKs Enable an Integrated Analog/Mixed-Signal/RF Design Tool Flow

- At top left is a bandgap circuit captured with Schematic Capture using symbols from the PDK
- Pcells are instantiated by Layout Editor with flight lines
- Cells are placed and wired to make final layout
- SPICE simulates extracted bandgap over temperature
Front-End Solution

- EDA Tools:
  - Schematic, Simulation Control, Multi-Level Circuit Simulation, Waveform Viewing
- Supported By:
  - Symbol libraries, SPICE Models, Callbacks
Back-End Solution

• EDA Tools:
  • Layout Editor, DRC, LVS, Parasitic Extraction

• Supported by:
  • Tech files, Rule decks, Parameterized Cells (Pcells)
Complete PDK-Based Analog/Mixed-Signal/RF Design Flow

Design Flow Manager

- SPICE Deck Generator
- Schematic Netlist
- Scripting Language
- LVS Netlist
- Parasitic Netlist

Schematic Driven Layout Directives

- Schematic Entry
- SPICE
- SPICE RF
- Mixed Signal
- Full Chip
- Parasitics
- Waveform Viewer
- Layout Editor
- Parasitics
- DRC
- LPE
- LVS
- C-Extract
- RC-Extract
- Reducer

Schematic Symbols
Netlist Equations
SPICE Models
Layout Technology File
PCELLS
DRC Rulefile
LVS Rulefile
Extract Rulefile

PDK

Front End Flow with PDK
Back End Flow with PDK
Silvaco PDK-Based Analog/Mixed-Signal/RF Design Flow
Gateway Schematic Editor and Analog/Mixed-Signal/RF Front-End

Front-end to hierarchical design with cross-probing, marching waveforms, analysis options, and optimization.

Mixes transistor and behavioral level (Verilog-A) schematics.
SmartSpice Circuit Simulator with SmartView

- Transient noise simulation with voltage and noise waveforms at 2 different circuit nodes.

- SmartSpice-64 simulates full chip power and signal integrity of extracted clock trees.

- SmartView produces annotated plots and graphs of measurements of time, voltage, current, and power for rise time, slope, vector calculator, and eye diagrams.
Expert Layout Editor Generates Parameterized Cells

- Full customizable hotkeys, macros, toolbars, layers, colors, and stipples can be directly imported.
- All-angle polygons for analog.
- High capacity loads over 10 gigabytes in minutes with fast panning and zooming.
Guardian DRC/LPE/LVS Verification

Intuitive graphical DRC error debugging in Expert.

Interactive hierarchical cross-probing of LVS discrepancy

Net Tracing follows nets and devices between layout and schematic.
Hipex-Full-Chip Parasitic Extractor Product Design Flow

Hipex-C provides detailed coupling capacitor netlists for accurate analyses of overlap, lateral, and fringe capacitances.

Hipex-RC supports SPICE, DSPF formats.
How do you Build a Good PDK?

- Silvaco process design kit (PDK) development services jump-starts analog and mixed-signal design teams and the CAD teams who support them with all of the foundry-specific models, symbols, rule decks and parameterized cells (P-cells) required for rapid, sustainable success using the complete Silvaco custom IC design toolset.

- Build it yourself using the following steps:
  - Write a specification
  - Collect the foundry documents
  - Build a front-end kit
  - Build a back-end kit
  - Verify the kit
  - Package the kit for distribution
  - Support the kit as process technology or EDA tools change
Foundry Design Documents for PDK Development

- Basic Level - Standard Foundry Documents
  - HSPICE Model
  - Layout Design Rules
  - DRC/LVS technology file

- Compatibility Level - standard PDK Kit for:
  - GDSII examples with layer map
  - Schematic symbol standard
  - Documentation from other PDKs
  - FSA Checklist

- PDK Development Accelerators
  - Script files from other PDKs
  - DRC/LVS testcase suite
PDK Front-end Deliverables

• Schematic Symbols – for the Gateway Schematic Editor invokes parameterized cells in the Expert Layout design tool that are DRC and LVS correct
  • These parameterized symbols and respective subcircuits are integrated and tested with the SPICE models to assure a standard convention for transistor level simulation
  • P-cells are written in the LISA Scripting Language.

• SPICE Models – SPICE model files verified with the SmartSpice Circuit Simulator at the foundry supplied process corners (temperature, voltage, process)
  • Silvaco can optionally extract a set of models from a wafer or measured data to produce a complete measured vs. simulation for each device
• Technology Files – layer files that correlate the legal GDSII layers for each of the process layers for layout and verification tools
  • Display files to customize the layout and schematic tools for GDS layers, display colors and user-customizable hot keys

• Rule Decks – contain the layout rules encoded into the format used by:
  • Expert Layout Editor
  • Guardian DRC /LVS/LPE tools
  • Hipex Full-chip Parasitic Extractor

• Parameterized Cells – enable annotated device schematics to be automatically drawn in the Expert Layout Editor, DRC and LVS correct, using the LISA scripting language
<table>
<thead>
<tr>
<th>Step</th>
<th>Foundry</th>
<th>Silvaco</th>
</tr>
</thead>
<tbody>
<tr>
<td>Deliver Foundry Data</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Extract SPICE Models</td>
<td></td>
<td>optional</td>
</tr>
<tr>
<td>Deliver Front-End Kit</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>(schematic symbols with SPICE models)</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Deliver Back-end Kit (DRC, LVS, LPE, Pcells)</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Design Review and Training</td>
<td>optional</td>
<td>✓</td>
</tr>
<tr>
<td>Validate PDK</td>
<td>optional</td>
<td>✓</td>
</tr>
<tr>
<td>Deliver Final PDK</td>
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<td>✓</td>
</tr>
<tr>
<td>Support Mutual Customers</td>
<td>optional</td>
<td>✓</td>
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</table>
## Data Format of Design Tool vs. Silvaco Compatibility

<table>
<thead>
<tr>
<th>Data Format of Design Tool</th>
<th>Silvaco Compatibility</th>
</tr>
</thead>
<tbody>
<tr>
<td>Schematics</td>
<td>EDIF 2 0 0 Import in Gateway</td>
</tr>
<tr>
<td>Layout Editor Tech Files</td>
<td>Expert reads Virtuoso™ files</td>
</tr>
<tr>
<td>Layout Data</td>
<td>Expert reads/writes GDSII</td>
</tr>
<tr>
<td>DRC/LVS Decks</td>
<td>Guardian translates Calibre™ and Diva/Dracula/Assura™</td>
</tr>
<tr>
<td>SPICE models</td>
<td>SmartSpice reads HSPICE™</td>
</tr>
<tr>
<td>SPICE netlists, commands</td>
<td>SmartSpice reads HSPICE™</td>
</tr>
</tbody>
</table>
How to you measure quality of PDK?
Other Industries Have the Same Problems

- 1924 – Federal Food and Drug Act prohibits untrue claims
- 1973 – Required on all foods with added nutrients or claims
- 1989 – New Rules
- 1993 – Label Finalized
- 1995 – 18 months later appears on all food packages

How to Read a Nutrition Facts Label

Macaroni & Cheese

<table>
<thead>
<tr>
<th>Nutrition Facts</th>
</tr>
</thead>
<tbody>
<tr>
<td>Serving Size: 1 cup (228g)</td>
</tr>
<tr>
<td>Serving Per Container: 2</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Amount Per Serving</th>
<th>% Daily Value*</th>
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</thead>
<tbody>
<tr>
<td>Calories: 250</td>
<td>Calories from Fat 110</td>
</tr>
<tr>
<td>Total Fat: 12g</td>
<td>18%</td>
</tr>
<tr>
<td>Saturated Fat: 3g</td>
<td>15%</td>
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<tr>
<td>Cholesterol: 30mg</td>
<td>10%</td>
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<tr>
<td>Sodium: 470mg</td>
<td>20%</td>
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<tr>
<td>Total Carbohydrate: 31g</td>
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<tr>
<td>Dietary Fiber: 0g</td>
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<tr>
<td>Sugars: 5g</td>
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</tr>
<tr>
<td>Protein: 5g</td>
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</tr>
</tbody>
</table>

Quick Guide to % DV

5% or less is Low
20% or more is High

Limit these Nutrients

Get Enough of these Nutrients

Footnote

*Percent Daily Values are based on a 2,000 calorie diet. Your Daily Values may be higher or lower depending on your calorie needs.

<table>
<thead>
<tr>
<th>Calories: 2,000</th>
<th>2,500</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Fat: Less than 65g</td>
<td>65g</td>
</tr>
<tr>
<td>Sat Fat: Less than 20g</td>
<td>25g</td>
</tr>
<tr>
<td>Cholesterol: Less than 300mg</td>
<td>300mg</td>
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<tr>
<td>Sodium: 2,400mg</td>
<td>2,400mg</td>
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<tr>
<td>Total Carbohydrate: Less than 300g</td>
<td>375g</td>
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<tr>
<td>Dietary Fiber: 25g</td>
<td>30g</td>
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# PDK Checklist – Foundry Process Documents

## Foundry Process Documents

<table>
<thead>
<tr>
<th>Document</th>
<th>Document Number &amp; Title</th>
<th>Section</th>
<th>Revision</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design Manual (Devices)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Electrical Parameters</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Design Layout Rules</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Spice Model</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RF Parameters/Modeling</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Noise Model</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Matching Models</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>ESD Guidelines</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DRC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LVS</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Parasitic Extraction</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Layer Map</td>
<td></td>
<td></td>
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</table>
## PDK Checklist – EDA Tool Support

<table>
<thead>
<tr>
<th>Type</th>
<th>Vendor and Tool</th>
<th>Version</th>
<th>Version Date</th>
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<tbody>
<tr>
<td>Schematic</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Simulation Control</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Circuit Simulator (A)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Circuit Simulator (B)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Circuit Simulator (C)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Circuit Simulator (D)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Layout Editor</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DRC Checker</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LVS Checker</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Parasitic Extractor</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Analysis Tools</td>
<td></td>
<td></td>
<td></td>
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</table>
### Device Types Supported by MS/RF Processes

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Examples of Devices of this Type</th>
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</thead>
<tbody>
<tr>
<td>MOS</td>
<td>NMOS/PMOS LV/HV, LVth/HVth, thick oxide, or floating gate</td>
</tr>
<tr>
<td>BJT</td>
<td>NPN/PNP, LV/HV, lateral, vertical</td>
</tr>
<tr>
<td>Diodes</td>
<td>N+/PW, P+/NW, Zener</td>
</tr>
<tr>
<td>Capacitors</td>
<td>poly-poly, MIM, tunnel, hi-Q</td>
</tr>
<tr>
<td>Resistors</td>
<td>n-diff, p-diff, n-well, poly0, poly1, polyn, fuse, and metal</td>
</tr>
<tr>
<td>Inductors</td>
<td>standard and differential</td>
</tr>
<tr>
<td>Varactors</td>
<td>MOS, junction, and hyperabrupt</td>
</tr>
<tr>
<td>-------------</td>
<td>-------------</td>
</tr>
<tr>
<td>MOS</td>
<td>mymos</td>
</tr>
<tr>
<td>BJT</td>
<td></td>
</tr>
<tr>
<td>Diode</td>
<td></td>
</tr>
<tr>
<td>CAP</td>
<td></td>
</tr>
<tr>
<td>RES</td>
<td></td>
</tr>
<tr>
<td>IND</td>
<td></td>
</tr>
<tr>
<td>VAR</td>
<td></td>
</tr>
</tbody>
</table>
- Enable Accurate Time Domain Analysis
- Accurate Passive Characterization of RC
- Accurate Analog/RF Models
  - High Frequency Noise
  - Low Frequency Noise - Flicker
  - Subckt Macro Models
  - RLC Passives
- Pcell Integrated Design Flow
  - Layout Editors and Pcells that can draw spiral Inductors
  - Extraction and Signal Integrity Analysis
Current Silvaco Foundry Partners

- TSMC
- UMC
- TOWERJAZZ
- ON Semiconductor
- MOSIS
- VIS
- FAB
- EPSON
- American Semiconductor Inc.
- amln
- Panasonic Analog Master Slice Service
- JRC
- GLOBALFOUNDRIES
• Delivered
  • 0.5u High Voltage 40V BCD/BiCMOS
  • 0.6u Mixed Signal 60V CMOS
  • 0.6u Mixed Signal 40V CMOS
  • 0.6u Mixed Signal 12V CMOS
  • 0.6u Mixed Signal CMOS
  • 0.18u RF CMOS
  • 1.25u Bipolar
  • MOSIS SCMOS

• In Development
  • 0.5u Mixed Signal CMOS
  • 0.18u SiGe
  • 1.5u 80V BCD
  • 0.13u RF CMOS
Summary: Silvaco PDK-Based Analog Design Flow

- **Single-Vendor Front-to-Back Solution**
  - Schematic entry front-end with complete set of circuit and mixed-mode simulators
  - Layout back-end with DRC/LVS/LPE and parasitic extraction
  - PDKs create integrated analog design tool flow

- **Easy Migration Path for Legacy Designs**
  - Industry-standard EDA formats and translator support

- **Foundries Support for Rapid Silvaco PDK Development**
  - PDK tightly links EDA tools, IC designers and foundries for optimal manufacturing success
  - Time-to-market for analog in CMOS

- **Affordable and Flexible Licensing**
  - Highest value, lowest risk, and best support