

3D Numerical Simulation of the Pseudo-MOS Transistor for SOI Film Characterization

D. Munteanu¹, S. Cristoloveanu¹ and E. Guichard²

¹LPCS/ENSERG, 23 rue des Martyrs BP 257, F-38016 Grenoble Cedex 1, France

²Silvaco Data System Sarl, 8, av. de Vignate 38610 Gières France

Introduction

The electrical characterization of SOI wafers is a difficult task due to the thinness of the film and complexity of the stacked structure. This is why the electrical properties are, in general inferred from the analysis of test MOS device or integrated circuits. Described below is a simple technique that takes advantage of the specific configuration of SOI and has the potential of being nondestructive. The pseudo-MOS transistor, also called the point-contact transistor or Ψ -MOSFET, is the first transistor that does not require any lithography or technology at all.

The Ψ -MOSFET is based on the inverted MOS structure that is inherent in all SOI materials. Figure 1 shows that the bulk-Si substrate can act as a gate terminal and can be biased to induce a conduction channel at the upper interface of the buried oxide.

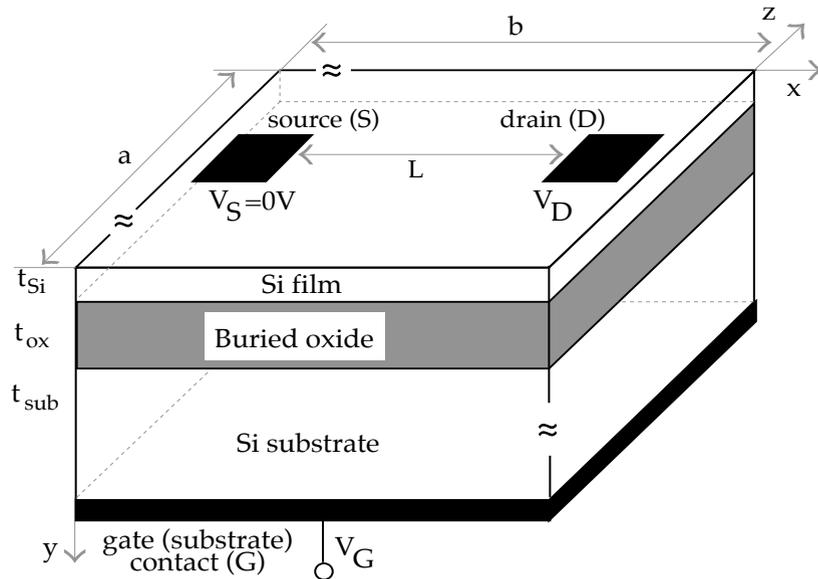


Figure 1. 3D structure used for simulation of Ψ -MOSFET.

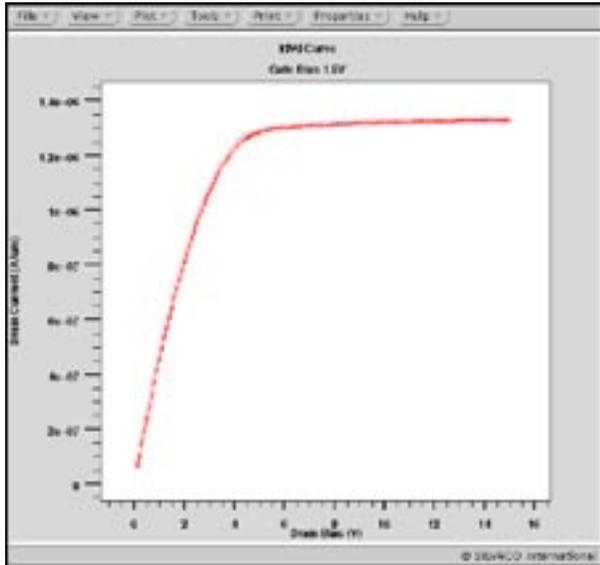


Figure 2. IdVd curve simulation of Ψ -MOSFET.

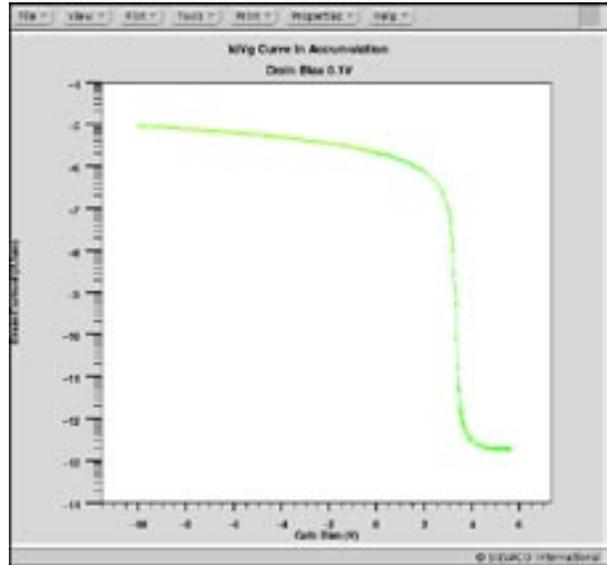


Figure 3. IdVg curve simulation of Ψ -MOSFET.

The buried oxide plays the role of a gate oxide and the Si film represents the transistor body. To operate the Ψ -MOSFET in situ (without lithography and metallization), low-pressure probes are placed on the silicon film and form source and drain point contacts.

Despite the device simplicity and nonparallelism of current lines, very pure MOSFET-like characteristics are produced. As shown in Figure 2, the simulated output $I_D V_D$ is very similar to a classical MOSFET curve.

Positive or negative biases can be applied to the gate to form accumulation or inversion channels at the interface.

For example a log $I_D V_G$ characteristic is shown for n-channel accumulation in Figure 3.

For all the reasons described above the Ψ -MOSFET stands as a unique method permitting a quick and complete evaluation of the electrical properties of SOI wafers prior to any device processing[1]. This article describes the use of 3-D numerical simulations which validate the method and show the optimum conditions for application and parameter extraction.

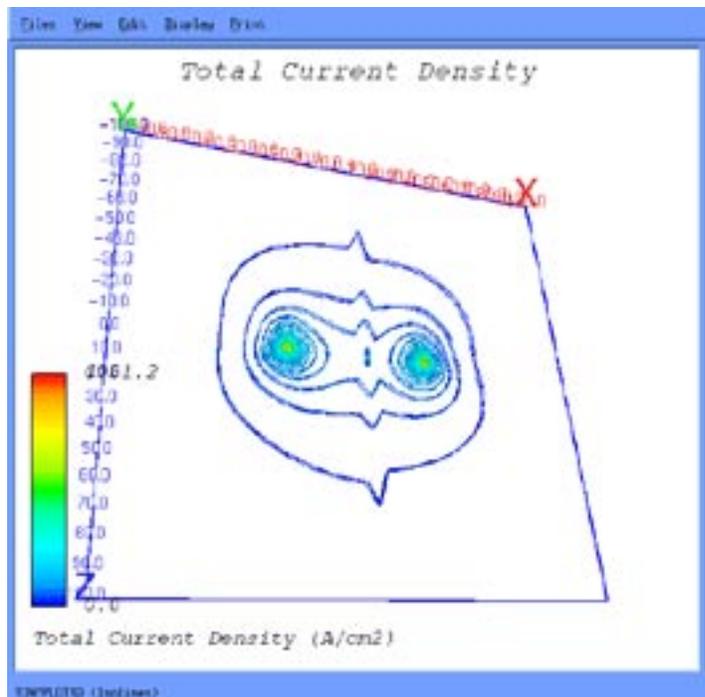


Figure 4. Current density lines (border-effect free structure) from **Device3D** simulation..

Structure Definition

The structure can be built either the internal syntax of **ATLAS** or **DevEdit3D** which allows interactive structure editing, structure specification and grid generation for 3D devices. The visualization of the structure is made with **TonyPlot3D** (Figure 4).

ATLAS is perfectly suited to this kind of simulation although it was developed for the simulation of fully processed devices. However special attention has to be paid the contact specification and especially to the determination of the work-function for the Schottky contact between the metal probe and the silicon film.

Simulation

ATLAS simulation calculates $I_D V_G$ and $I_D V_D$ characteristics for both inversion and accumulation channels in either n- or p-doped films (Figure 5). In addition, the simulations offer the distribution of the charge, potential (Figure 7) and electric field. The accuracy

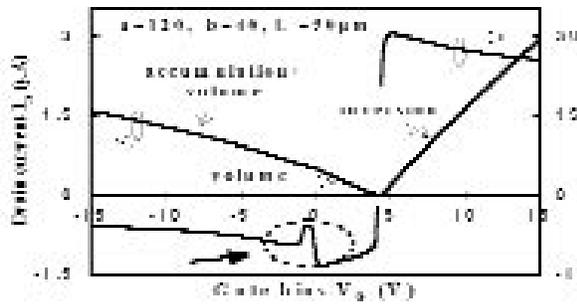


Figure 5. Simulated $I_D(V_G)$ and $gm(V_G)$.

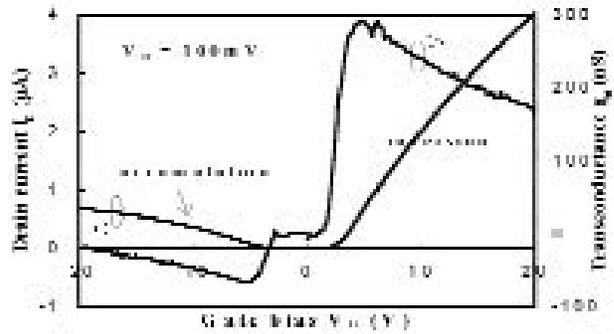


Figure 6. Experimental Ψ -MOSFET curves in a p-type UNIBOND

of the simulations has been validated by comparison with systematic experimental data (example in Figure 6) and by a self-consistent procedure: standard parameter extraction from the simulated curves and coherence of the output parameters with those initially fed into the simulator (carrier mobility, doping, oxide charges).

These simulations deliver illuminating information on the influence of several key parameters (film and substrate doping, film and buried oxide thickness, Schottky contact depth, series resistances, interface roughness).

More complex experimental situations have also been reproduced successfully:

- In a narrow range of gate voltages, a *depletion region* forms underneath the buried oxide. The depletion capacitance apparently modifies the oxide capacitance and gives rise to a hump in the drain current and transconductance (dotted circle in Figure 5). This hump can be used to evaluate the substrate doping.
- In accumulation, the current flows not only at the interface but also in the *film volume*. The simulations allow to make distinction between these two components as a function of film doping and thickness.

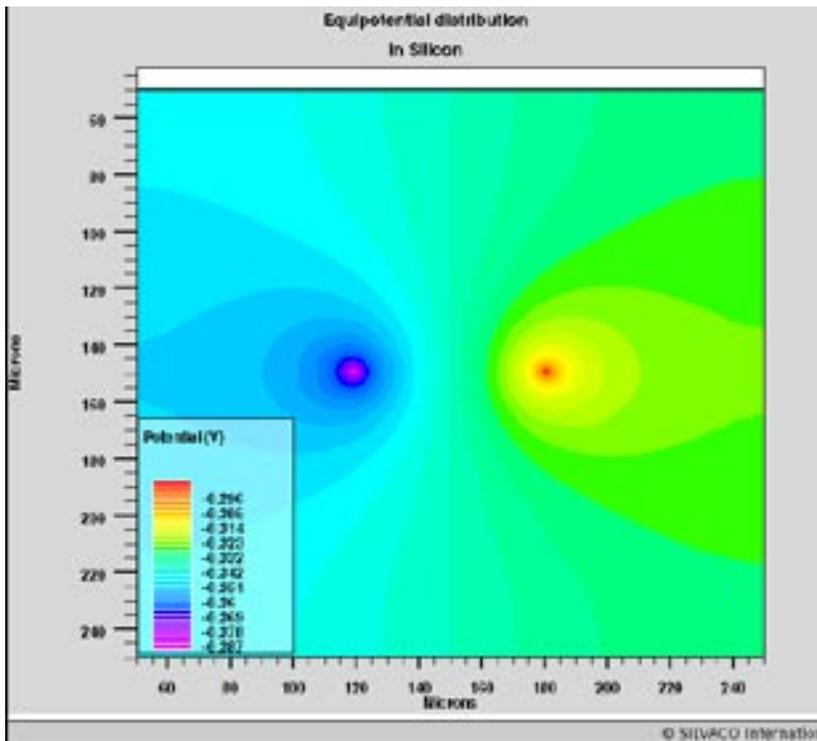


Figure 7. Equipotential line distribution in a $240 \times 240 \mu\text{m}^2$ sample.

A practical concern with the Ψ -MOSFET technique is the *geometrical factor* f_g which replaces the transistor aspect ratio, W/L , and is not known a priori. This factor is estimated experimentally by the comparison between the Ψ -MOSFET and 4-point probe data [1]. Any uncertainty directly impacts on the extraction accuracy of the carrier mobility and threshold voltage.

3-D simulations do show the non-parallel current flow lines across the sample (Figure 4). We verified that, in samples large enough when compared to the probe interdistance, the geometrical factor is roughly $f_g \approx 0.7$ in full agreement with the experiment.

A typical problem which can be solved using 3-D simulations is the influence of the *sample size* and the *proximity of the borders*. The investigation was conducted by either shrinking the sample size or by placing the contacts closer

to the edges. In both cases, the resulting distortion of the field distribution (Figure 8) is responsible for an apparent degradation of the transconductance (Figure 9), and hence extracted mobility (Figure 9), and hence extracted mobility.

On the other hand, when the probe interdistance becomes comparable with the contact area (Figure 10) the short-channel/large-contact effect causes an over-estimation of the carrier mobility.

In order for the SOI material quality not to be underestimated or over estimated it is therefore necessary to respect certain rules in term of probe inter-distance on sample size.

Conclusion

The 3D simulator Device3D has reliably modeled the Ψ -MOSFET structure. The simulations have uncovered a number of non-obvious features of Ψ -MOS transistor behavior. This work makes clear the conditions required for reliable operation of the Ψ -MOSFET for SOI substrate characterization.

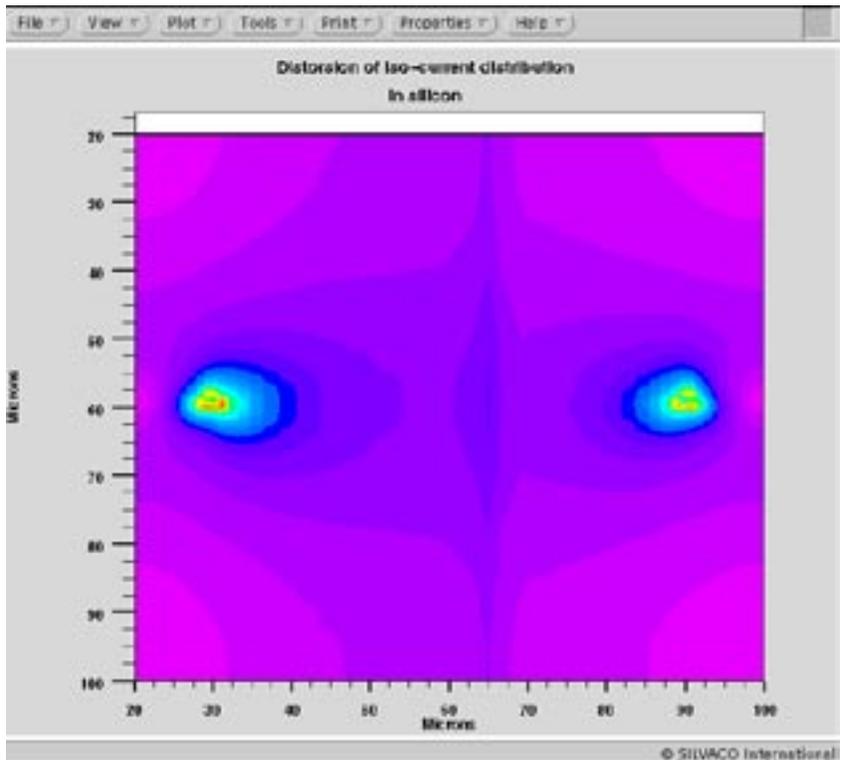


Figure 8. Border proximity effect shown by distortion of iso-current distribution.

References

- [1] S. Cristoloveanu, S. S. Li, Electrical Characterization of SOI Materials and Devices, Kluwer, (1995).
- [2] Atlas User's Manual, (1997).

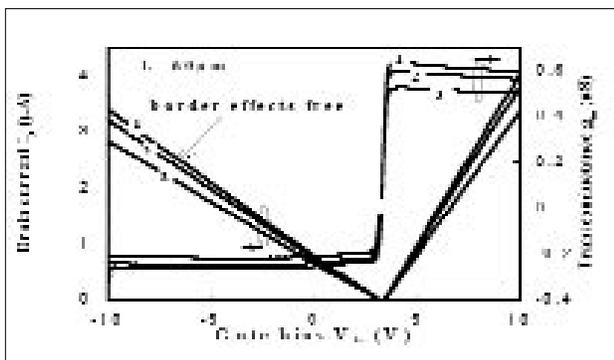


Figure 9. Simulated Ψ -MOSFET curves for different sample areas: (1) 200x200, (2) 120x120, (3) 80x80 μm^2 .

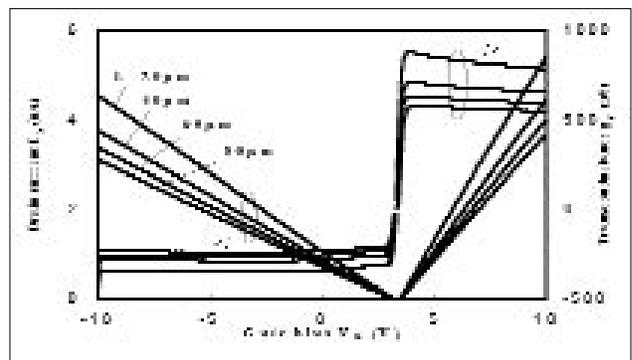


Figure 10. Influence of the 2-probe interdistance; 200x200 μm^2 sample, constant carrier mobility.