High-Performance Split-Gate Enhanced UMOSFET With p-Pillar Structure

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Abstract—In this paper, a split-gate resurf stepped oxide (RSO) vertical UMOSFET with p-pillar under the p\textsuperscript{+} plug region structure is proposed. The p-pillar could modulate the electric field of the drift region with the split-gate in 3-D and simultaneously brings electric field peaks at the sidewall junction between p-pillar and n-drift region. So the split-gate enhanced with p-pillar (SGEP) UMOS could increase the drift region doping concentration, reduce the on-state-specific resistance, and maintains the breakdown voltage as compared with the super junction and split-gate RSO UMOSs. Numerical simulation results show that the charge imbalance endurance of SGEP is also largely increased.

Index Terms—Breakdown voltage (BV), on-state specific resistance (RSP), split-gate, trench gate UMOSFET.

I. INTRODUCTION

In order to achieve the best trade-off between the breakdown voltage (BV) and specific on-state resistance ($R_{SP}$) for the vertical discrete power MOSFETs, a variety of solutions are proposed. Most of these solutions are based on the RESURF action of split-gate resurf stepped oxide (SG-RSO) along the drift region or super junctions (SJ) [1]–[5].

For the SG-RSO structure, it enhances the lateral depletion and allows the n-drift region doping concentration ($N_D$) to be increased. Moreover, the split-gate field plate between the gate and the drain reduces the Miller charge ($Q_{GD}$). The SG-RSO UMOS has a lower $R_{SP}$ as compared with the SJ UMOS at the low voltage range because of the higher doping concentration in the n-drift region, but not at the higher voltage range because the electric field distribution in the drift region for SG-RSO UMOS is not as uniform as that of SJ UMOS [3], [5].

In this paper, a p-pillar is adopted in the SG-RSO UMOS drift region under the p\textsuperscript{+} plug region. The p-pillar and split-gate could modulate the electric field of the drift region in 3-D simultaneously. In addition, the p-pillar also brings electric field peaks at the sidewall junction between p-pillar and n-drift region. So the split-gate enhanced with p-pillar (SGEP) UMOS could increase the $N_D$ and maintains the BV as compared with the SJ and SG-RSO UMOSs. Section II describes the device structure and operation concept. Section III gives the fabrication procedure. Section IV exhibits the results of the 3-D numerical simulation for comparing among SJ, SG-RSO and SGEP UMOSs, and the impact of p-pillar to SGEP UMOS characteristics. Section V concludes this paper.

II. DEVICE STRUCTURE AND OPERATION CONCEPT

A simplified 3-D view of the SGEP UMOS cell under consideration is shown in Fig. 1(c). Compared with the cells of the SJ UMOS and the SG-RSO UMOS as shown in Fig. 1(a) and (b), respectively, the SGEP UMOS contains the p-pillar under the p\textsuperscript{+} plug region, and the top-view size of the p-pillar is controlled by the hole contact ($2T \times 2W$).

Fig. 2 shows the electric field distribution of (a) the SJ and (b) the SG-RSO UMOSs as BV is 136 V with the same dimensions (given in Table I). In addition, the cut section 1(c) and cut section 2(d) from the breakdown points of the SJ and SG-RSO UMOSs are shown. Here, the field oxide and the split-gate electrode are hidden in cut section 2. In the SJ UMOS, the electric field peak and the BV point happen in the middle drift region of the junction between the n-pillar and p-pillar, the electric field distribution in the y-axis direction is almost uniform, but the electric field decreases sharply as the position is far away from the BV point in the x-axis direction.

In the SG-RSO UMOS, the electric field peak and the BV point happen in the corner of the split-gate electrode; the main drawback is that the lowest electric field exits in the middle of n\textsuperscript{−} drift region in the y-axis direction, so the SG-RSO UMOS has the worse characteristics than the SJ UMOS as BV is > 100 V [3].

Manuscript received February 20, 2013; revised April 21, 2013; accepted April 24, 2013. This work was supported in part by the Program for New Century Excellent Talents in University under Grant NCET-10-0052, Key Grant Project of Chinese Ministry of Education under Grant 313017, and the Specialized Research Fund for the Doctoral Program of Higher Education under Grant 20122304110016. The review of this paper was arranged by Editor G. Dolny.

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Digital Object Identifier 10.1109/TED.2013.2260547
From the illustration of SJ and SG-RSO UMOSs, we know that the improvement could be achieved by increasing the electric field in the middle of n-drift region. In other words, the doping concentration in n-drift region could be increased by reducing the mesa width of the SG-RSO or n-pillar width of the SJ [5]. However, the narrow mesa would add the difficulty in the fabrication, especially in the metal trench contact. The SJ UMOS could overcome this by the orthogonal gate layout [12], but it is not suitable for the SG-RSO UMOS. Although the proposed SG-RSO UMOS could solve this issue by adopting a p-pillar under the source electrode and thus not increasing the manufacture difficulty, the p-pillar could enhance the RESURF effect to the n-drift region, so the drift region doping can be substantially increased and still keeping the same breakdown voltage. With the SG-RSO UMOS structure, the proposed SGEP UMOS with p-pillar could modify the electric field distribution in the n^-drift region effectively. At the off-state, the p-pillar could bring another two electric field peaks at the vertical interfaces of n-/p-pillar in the middle of drift region, as shown in the SGEP UMOS cell, while they are far away from the electric field peak at the corner of split-gate electrode, avoiding the composition of them. Then at the same BV, the SGEP UMOS could have the higher n^-drift doping concentration and the lower R_sp compared with the SJ and SG-RSO UMOSs.

III. FABRICATION PROCEDURE

Fig. 3 shows the fabrication process steps for the SGEP UMOS. It is similar to the methods used to fabricate the SG-RSO UMOS until the forming of the p-pillar. We start with an n^+ wafer and grow the n-epilayer, this layer forms the drift region of the device. Over this layer, a sacrifice oxide is grown and after the p-type ion implanting for the channel, the p-pillar trench is opened (Mask 1) (a). A p-type (boron doped) layer is epitaxially grown to fill the trench using the anisotropic epitaxial growth with SiH2Cl2 (DCS) and HCl gases [6] over the surface of n-epilayer, then the trench filled with p-pillar is formed with etching and chemical-mechanical polishing (CMP). The CMP process is adopted to remove the sidewall structure in the epitaxy process (b). Then the gate trench is opened (Mask 2) (c). The sacrificial oxide is grown, then etched off to remove the damaged surface of the trenches and to smooth the trench corners. Thick oxide and n-type poly are deposited in the trenches. Following two materials are etched back such that the p-doped region could be explored completely (d). The gate oxide is thermally grown, and the isolated oxide between gate and split-gate is formed simultaneously. The gate poly layer is deposited to fill the trench and etched back (e). After n^+ ion implanting for the source region and gate poly, an oxide layer is deposited, and the hole contact is opened (Mask 1 is used again). After implanting the p^+ ion for the p^+ plug region, the oxide on the silicon surface is removed (f). Aluminium is deposited on the front and backside of the substrate, respectively, and then etched to define the source and drain electrodes (g). In this process, it reduces the cost of the fabrication procedure for the photo masks of p-pillar and contact hole is the same one. In addition, the rapid thermal anneal is adopted in the most anneal processes for reducing the impact of interdiffusion between phosphorus in the n^-drift region and boron in the p-pillar.

IV. RESULTS AND DISCUSSION

To investigate the improvement of the SGEP UMOS, we present an extensive analysis of the device in contrast with the SJ, SG-RSO UMOSs with the same structure as the width of the half cell is 2.4 μm, and design the BV of the three UMOSs 136 V with the structures details given in Table I. Using 3-D numerical simulations performed by VICTORY Process Cell, DEVEDIT3D and ATLAS simulators [7]–[9], considering the models of bandgap narrowing, concentration dependent, parallel electric field dependence, and Shockley Read Hall. The results show that the researched device exhibits improved drive current, R_sp, and charge imbalance characteristics.

A. Off-State Characteristics

Fig. 4 shows the BV comparing of the SJ, SG-RSO, and SGEP UMOSs, and the breakdown limit of drain current density is selected as \( 1 \times 10^{-10} \) A/μm². Here, the BV of SJ and SGEP UMOSs is 136 V, and the BV of SG-RSO UMOS is 138 V. The potential contours comparing of the SJ, SG-RSO, and SGEP UMOSs at \( V_{GS} = 0 \) V and \( V_{DS} = 136 \) V are shown in Fig. 5. The potential density of the SGEP UMOS is increased in the n^-drift region. As the electric field...
distribution of the SGEP UMOS shown in Fig. 6, the lower electric field location of the drift region is separated by the p-pillar in the SGEP UMOS compared with that of the SG-RSO UMOS. And the p-pillar brings two electric field peaks at the vertical interfaces of junction between the n− drift region and p-pillar, as the electric field distribution of cut section 4 shown. While not as the corner of the sidewall trench in the SG-RSO UMOS [10], the breakdown point in the SGEP UMOS has shifted to the p/n junction near the corner of the split-gate electrode, where the electric field is affected by the split-gate electrode and the p-pillar simultaneously. The device breaks down when the n− drift region is depleted completely and the critical electric field occurs between the p-pillar and n− drift region in the z-axis direction.

### B. On-State Characteristics

Fig. 7 shows the $I_{DS} - V_{DS}$ characteristics comparing of the SJ, SG-RSO, and SGEP UMOSs as $V_{GS}$ is 3, 4, 5, and 10 V, respectively, depicting the higher drive current in the SGEP UMOS compared with the SJ and SG-RSO UMOSs for all bias conditions. The $R_{SP}$ of the device is the ratio of applied $V_{DS}$ to the resulting $I_{DS}$ in the linear region of operation, multiplies the active area, and it varies with the applied $V_{GS}$ [11]. The $R_{SP}$ evaluated at $V_{DS} = 0.2$ V, as a function of gate voltage for the SGEP UMOS in contrast to the SJ and SG-RSO UMOSs, is shown in Fig. 8 at the left y-axis. As expected, the SGEP UMOS shows lowest $R_{SP}$ compared with the SJ and SG-RSO UMOSs. The figure also shows the percentage improvement in the $R_{SP}$ of the device in the right y-axis; the SGEP UMOS...
Fig. 7. $I_D$–$V_{DS}$ characteristics comparing of the (a) SJ, (b) SG-RSO, and (c) SGEP UMOSs as $V_{GS}$ is 3, 4, 5, and 10 V, respectively.

Fig. 8. $R_S$ as a function of gate voltage (left $y$-axis) with $V_{DS} = 0.2$ V. The percentage reduction in $R_S$ (right $y$-axis) compared with the SJ and SG-RSO UMOSs, respectively.

Fig. 9. Relationship between BV and the dimensions of the p-pillar for the SGEP UMOS.

Fig. 10. Relationship between BV and the doping concentration.

Fig. 11. Relationship between BV and the doping concentration.

The percentage reduction in $R_S$ by higher than 30% and 43% compared with the SJ and SG-RSO UMOSs respectively. The percentage improvement increases with the $V_{GS}$.

C. Charge Imbalance Characteristics

Fig. 9 shows the relationship between the BV and the doping concentration for the SJ, SG-RSO, and SGEP UMOSs. In the SGEP UMOS, the charge imbalance condition has changed in the local super junction structure that the doping concentrations of p-pillar and n$^-$ drift region are not equal because the split gate and the p-pillar are depleting the n$^-$ drift region simultaneously. The SJ UMOS reaches the maximum BV as $N_D$ is $1.6 \times 10^{16}$ cm$^{-3}$, and the SG-RSO UMOS reaches the maximum BV as $N_D$ is $8.0 \times 10^{15}$ cm$^{-3}$, while the SGEP UMOS gets the maximum BV as $N_D$ is $4.7 \times 10^{16}$ cm$^{-3}$. Here, we define the charge imbalance endurance (CIE) is the discrepancy of doping concentration ($\Delta N$) as BV is higher than 100 V. Then, the CIE of SJ UMOS $\Delta N_{SJ-n}$ is $1.2 \times 10^{16}$ cm$^{-3}$, the CIE of SG-RSO UMOS $\Delta N_{SG-RSO-n}$ is $1.5 \times 10^{16}$ cm$^{-3}$, while the CIE of SGEP UMOS $\Delta N_{SGEP-n}$ is $1.9 \times 10^{16}$ cm$^{-3}$, $3.1 \times 10^{16}$ cm$^{-3}$, respectively. Therefore, it could be stated that the SGEP UMOS has the better charge imbalance endurance than the SJ and SG-RSO UMOSs.

D. p-Pillar Dimensions Characteristics

The relationship of the BV to p-pillar dimensions in the SGEP UMOS is shown in Fig. 10. The p-pillar dimensions impact the breakdown point occurring whether at the junction between p-body and n$^-$ drift region (p-body/n) or between p-pillar and n$^-$ drift (p-pillar/n). The RESURF action of split gate and the p-pillar could not deplete the n$^-$ drift region completely as the width of p-pillar ($W$) is <0.55 $\mu$m, as shown in Fig. 11(a) and (c), and the breakdown point occurs at the p-body/n junction. The RESURF action effect is enhanced excessively as W is higher than 0.55 $\mu$m, so the breakdown point occurs at the p-pillar/n junction in the x-axis direction as shown in Fig. 11(b) and (d). Similar to the impact of p-pillar
Fig. 11. Electric field distribution of the SGEP UMOS with (a) $W = 0.35 \, \mu m$ and (b) $W = 0.75 \, \mu m$. The 3-D electric field distribution from (c) cut section 1 and (d) cut section 2 extracted from (a) and (b), respectively.

Fig. 12. Electric field distribution of the SGEP UMOS with (a) $T = 0.3 \, \mu m$ and (b) $T = 0.7 \, \mu m$. The 3-D electric field distribution from (c) cut section 1 and (d) cut section 2 extracted from (a) and (b), respectively.

width, the breakdown point occurs at the p-body/n junction as the thickness of the p-pillar ($T$) is $< 0.5 \, \mu m$, but it also occurs at the p-pillar/n in the z-axis direction when $T$ is $> 0.5 \, \mu m$, if the charge in the n$^-$ drift region could not compensate for that in the p-pillar, as shown in Fig. 12. The BV, however, increases with the depth of the pillar ($H$), because the charge mismatch effect is enhanced with the $H$ decreasing.

The performance of SGEP UMOS is compared with the ideal silicon limit, SJ, OB, GOB [3], and SOB [13] UMOSs. From Fig. 13, we can see that SGEP has the best performance over OB, SOB, and GOB UMOSs in the 100–200 breakdown voltage range. This can be explained, for the higher voltage range, the electric field distribution in the bottom of the drift region in SOB UMOS is lower than that of OB and GOB UMOSs, and the breakdown voltage point also occurs at the corner of the sidewall trench, which limits the breakdown voltage performance for SOB UMOS. Although the double RESURF effects of split gate and p-pillar enhance the performance of SGEP UMOS, it is difficult for SGEP UMOS to be fabricated at a breakdown voltage $< 100 \, V$ because of the small size of the p-pillar. For a voltage $> 220 \, V$, the SGEP structure shows the higher $R_{SP}$ because the oxide thickness becomes larger than the drift region width at a higher breakdown voltage and thus requires a larger device area, whereas the width of the p-pillar in the SJ UMOS is equal to the n-pillar width.

V. Conclusion

In this paper, a split-gate enhanced with p-pillar in the drift region under the p$^+$ plug region UMOS was proposed. Moreover, the improved structure was verified by numerous simulations. According to the results, a SGEP with 136 V and $45 \, m\Omega \cdot mm^2$ was achieved. The p-pillar modulated the electric field distribution, brought electric field peaks at the interfaces of junctions between p-pillar and n$^-$ drift region, increased the n$^-$ drift region doping concentration, and reduced $R_{SP}$. The simulation results showed that the SGEP UMOS improved the $R_{SP}$ higher than 30% and 43% compared with SJ and SG-RSO UMOSs respectively, enlarged the drive current, and increased the charge imbalance endurance.

REFERENCES


Authors’ biographies and photographs not available at the time of publication.