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FAST TRACK COMMUNICATION

Improved vertical MOSFET performance using an epitaxial channel and a stacked silicon-insulator structure

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Abstract
A vertical MOSFET (VMOST) incorporating an epitaxial channel and a drain junction in a stacked silicon-insulator structure is presented. In this device structure, an oxide layer near the drain junction edge (referred to as a junction stop) acts as a dopant diffusion barrier and consequently a shallow drain junction is formed to suppress short channel effects. To investigate the scalability of this device, a simulation study in the sub-100 nm regime calibrated to measured results on the fabricated devices is carried out. The use of an epitaxial channel delivers 50% higher drive current due to the higher mobility of the retrograde channel and the junction stop structure delivers improvements of threshold voltage roll-off and drain-induced barrier lowering compared with a conventional VMOST.

(Some figures may appear in colour only in the online journal)

The emerging three-dimensional (3D) integration technology has received much attention as a viable solution to extend a fundamental limit of CMOS scaling because 3D technologies allow reducing chip size, delay time in interconnections and power dissipation [1]. In order to fully benefit from the 3D architecture, the development of vertical MOSFETs (VMOSTs) is essential. Some prototype VMOSTs for memory and RF applications have been reported already [2–5]. VMOSTs have several advantages over conventional MOSTs. Firstly, short channel lengths can be achieved without the requirement for advanced lithography. Secondly, thin pillar double-gate VMOSTs have been recognized as being promising for future CMOS because of high current drive [4]. Finally, p-VMOSTs offer the prospect of around 50% higher drive current than planar p-MOSTs, because the hole mobility on the (1 1 0) pillar side plane is higher than that on the (1 0 0) planar surface [6]. The drawbacks of VMOSTs are associated with the difficulty of channel length control and channel engineering to suppress short channel effects. Several approaches have been proposed to improve short channel effects in VMOSTs. A thin pillar double-gate structure is one approach, but the fabrication of the drain contact requires complicated processing [7] and their device performances could deteriorate from depletion isolation effect [8]. To address this problem, a new concept of junction stop (JS) has been proposed [9], which incorporates an oxide barrier layer near the drain junction edge. Simulation studies indicate that the JS could suppress short channel effects in a sub-100 nm device even with a uniform channel doping profile [10]. The JS-VMOSTs have been fabricated by different fabrication processes [5, 11]. However, no results have yet been reported on the short channel effects in the epitaxial channel JS-VMOSTs because many devices with different channel lengths are necessary to evaluate channel length dependence of device parameters.

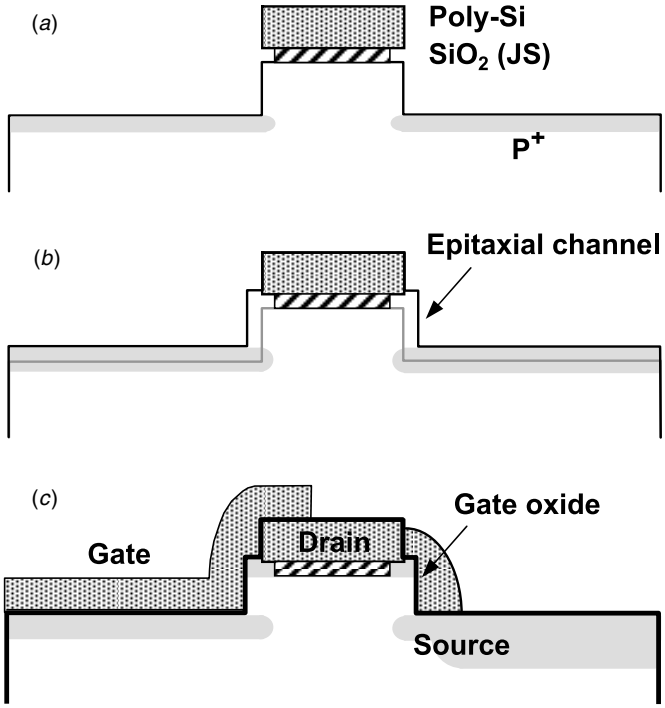

Figure 1. Main process steps of a JS-VMOST with an epitaxial channel: (*a*) formation of a stack of poly-Si and oxide layers, followed by dry etch to form a pillar, boron implantation to form a shallow source junction and HF wet etch to form undercuts on the pillar sidewalls; (*b*) Si epitaxy for the undoped channel; (*c*) gate oxidation, gate spacer formation and boron implantation to form a deep source junction. A poly-Si liner extends to one side of the gate spacers for the gate contact.

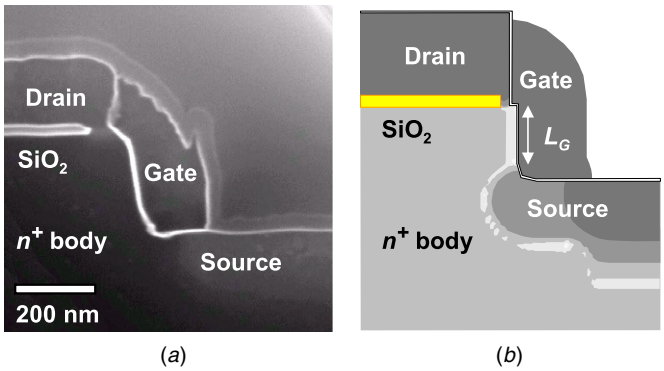

Figure 2. (*a*) Cross-sectional SEM image of the JS-VMOST after junction stain etch; (*b*) a corresponding simulated device structure.

In this paper, we investigate short channel effects in the epitaxial channel JS-VMOSTs. Simulations, calibrated to experimental data, show that the epitaxial channel increases the drain current and the JS structure delivers improved threshold voltage roll-off and drain induced barrier lowering (DIBL).

Figure 1 shows the schematic diagrams of device fabrication process steps for the JS-VMOST. After the deposition of a 200 nm thick poly-Si layer on a 20 nm thick thermally grown oxide, the pillar was formed using an anisotropic dry etch. A shallow source junction was formed by boron ion implantation at a dose of 2×10^{14} cm^{-2} and an energy of 5 keV. The oxide layer was then etched by dilute hydrofluoric acid to create a 20 nm width undercut beneath the poly-Si layer. This undercut provides seeding of the Si epitaxial growth between the poly-Si layer and the Si pillar. Subsequently, a 20 nm thick undoped epitaxial channel was grown by LPCVD. The space between the poly-Si and the Si pillar over the oxide barrier was filled with the Si epitaxial layer. A 3 nm thick gate oxide growth was followed by the poly-Si deposition. The poly-Si sidewall spacer was formed by a highly selective anisotropic poly-Si etch with a photoresist layer. A boron ion implantation at a dose of 4×10^{15} cm^{-2} and an energy of 15 keV was then carried out for doping of the poly-Si gate and the poly-Si drain, and the formation of the deep source junction. Finally, a rapid thermal anneal (RTA) at 1000 °C for 20 s was performed. During the RTA, boron out-diffusion from the poly-Si drain creates a shallow drain junction near the JS.

Figure 2(*a*) shows a cross-sectional SEM image of the fabricated JS-VMOST. It is clear that the poly-Si drain contact is in contact with the Si pillar. The indentation on the pillar side adjacent to the JS is caused by a slower Si growth rate on the poly-Si than on the single crystal Si. Secondary ion mass spectroscopy (SIMS) analyses show that the n^+ body has reasonably uniform doping profile over a depth of 0.6 μm with doping concentration of 1×10^{18} cm^{-3}. Figure 2(*b*) shows a corresponding simulated device structure created by ATHENA [12] which was calibrated by reference to SEM images and SIMS profiles. The simulated carrier concentration is shown by grey scales, and the white region between source and drain indicates that this device has a retrograde channel.

Process simulations were carried out in accordance with the process steps shown in figure 1. The Si epitaxy step was primarily adjusted because the growth rates on single crystal Si and poly-Si regions were different. After the Si deposition, the Si film on the poly-Si region was removed. Device simulations were carried out using ATLAS with Boltzmann statistics, concentration-dependent mobility model, a Shockley–Read–Hall lifetime model and bandgap narrowing [12]. The default parameter values were employed for the simulations. The best fit to the measured characteristics was obtained for a retrograde channel with surface concentration of 7×10^{16} cm^{-3}.

Figure 3 shows measured output characteristics of the JS-VMOST together with simulated results. The channel length (L_G) determined by junction staining and SEM cross-sectional images is 190 nm. The fabricated p-VMOST ($L_G =$ 190 nm) gives a drive current of 12 μA μm^{-1}, which is about three times larger than the value of 3.8 μA μm^{-1} reported by Jayanarayanan *et al* [11] for a p-VMOST ($L_G = 50$ nm) and similar to our previous work [5] for a n-VMOST ($L_G =$ 70 nm). Here, the drive current is defined as the drain current at $V_D = V_G - V_T = \pm 1$ V. However, the drive current is lower than advanced double-gate MOSFETs [4, 7]. The lower drive current is mainly attributed to the high parasitic source/drain resistance and this problem could be solved either by using silicidation or a top drain contact structure.

To investigate short channel effects in the JS-VMOST, figure 4(*a*) shows a comparison of the simulated threshold voltage roll-off behaviour of the JS-VMOSTs and the

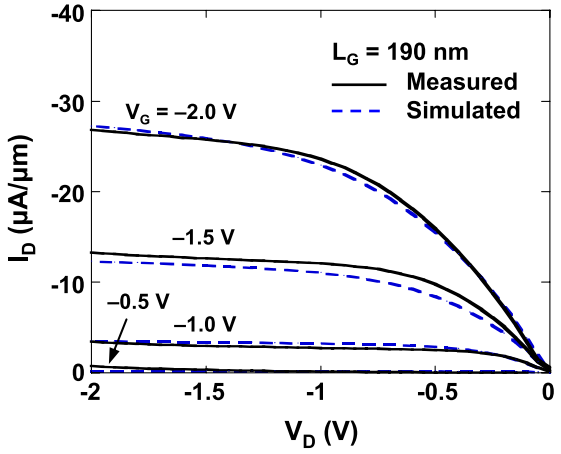

Figure 3. Measured and simulated output characteristics of the JS-VMOST ($L_G = 190$ nm).

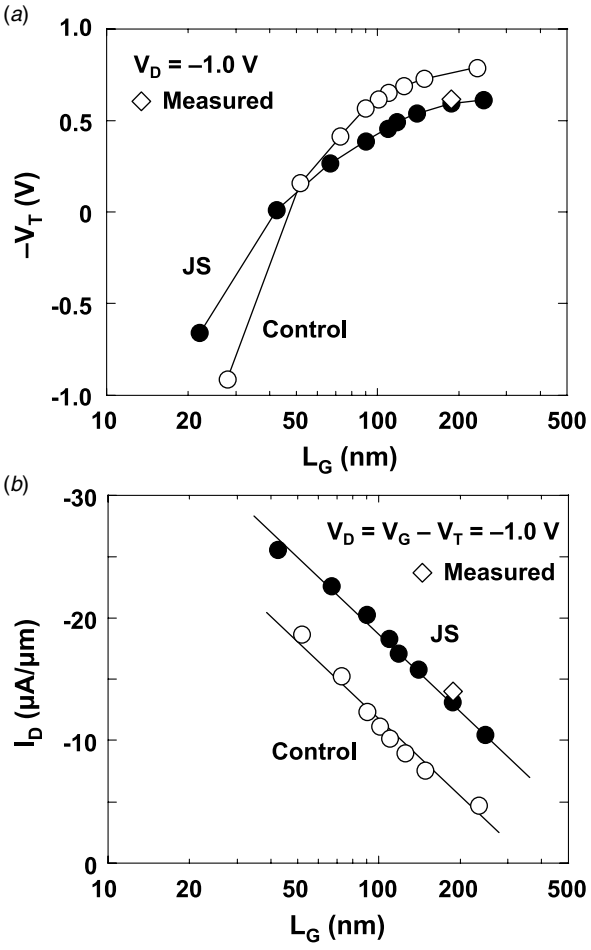

Figure 4. (*a*) The simulated threshold voltage roll-off behaviour at $V_D = -1$ V of the JS-VMOSTs and the conventional VMOSTs. The measurement result is also included; (*b*) simulated drain current as a function of channel length of the JS-VMOSTs and the conventional VMOSTs at $V_D = V_G - V_T = -1$ V. The measurement result is also included.

conventional VMOSTs, with the latter being equivalent to devices without the JS. The JS is effective in suppressing short channel effects in spite of the lower threshold voltage. This improvement is a result of the reduced charge sharing in the

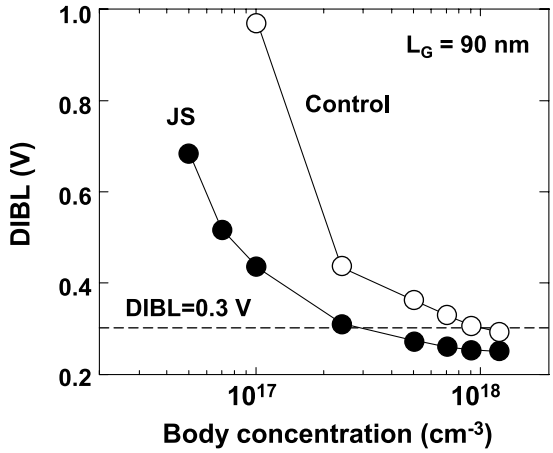

Figure 5. Simulated DIBL as a function of the body doping concentration of the JS-VMOSTs ($L_G = 90$ nm). For comparison, the results of the conventional VMOSTs are also shown. The DIBL values are evaluated from the gate voltage shift in the subthreshold characteristics between $V_D = -1$ V and -0.1 V, where the gate voltage is defined at $I_D = -1$ μA μm^{-1}.

drain depletion region associated with the effective formation of a shallow drain junction. The JS dramatically reduces the area of contact between the poly-Si drain and the n^+ body and consequently mitigates the encroachment of the electric field from the poly-Si drain. The shallow drain junction near the JS behaves in a similar way to the shallow drain extension in a conventional MOST. To investigate the scalability of the drive current, figure 4(*b*) shows the simulated drain current as a function of channel length. The JS-VMOST has around 50% higher drain current than the conventional VMOST in the sub-100 nm regime because of the retrograde channel profile.

To further investigate the effect of the channel doping profile on the *I–V* characteristics of the JS-VMOSTs, DIBL as a function of body doping concentration is simulated for the JS-VMOSTs and the conventional VMOSTs with $L_G =$ 90 nm. Here, the DIBL values are evaluated from the gate voltage shift in the subthreshold characteristics between $V_D = -1$ V and -0.1 V, where the gate voltage is defined at $I_D = -1$ μA μm^{-1}. Figure 5 shows that DIBL increases with decreasing body doping concentration for both devices. As for the JS-VMOST, a reasonable DIBL value less than 0.3 V can be obtained for a body doping concentration down to 2.5×10^{17} cm^{-3}, whereas this value of DIBL can be achieved at a body doping concentration over 1×10^{18} cm^{-3} for the conventional VMOST. A lower body doping concentration is advantageous because a higher drain current can be achieved due to decreased carrier scattering in the channel.

In summary, VMOSTs with an epitaxial channel and a JS structure have been successfully fabricated and short channel effects have been investigated by process and device simulations which are calibrated with the experimental data. The simulation study shows that the epitaxial channel increases the drive current due to the high carrier mobility in the retrograde channel, and the JS structure brings benefits in suppressing short channel effects due to the formation of a shallow drain junction.

Acknowledgments

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