# Predicting Capacitance Coupling of IPS Mode TFT-LCD Using CLEVER

## Introduction

Increasing demand for TFT-LCDs necessitates increasing display size and resolution. The narrowing of viewing angle and image degradation due to the electrical coupling between the data bus line and display electrodes called “crosstalk” creates serious problems. The in-plane switching (IPS) mode has been known as an excellent technology for realizing a extremely wide viewing angles. But the IPS-mode TFT-LCD has the drawback of lower aperture ratio when compared to the twist nematic (TN)-mode TFT-LCD when the pixel size is larger than 140 dots per inch(1).

If the electrode structure of IPS is not properly designed, it will result in a small aperture ratio and a visible crosstalk. It is well known that the crosstalk caused by parasitic capacitive coupling between driving electrodes and data-bus lines could result in image degradation. The crosstalk can be reduced by a thick dielectric film such as SiNx between the data-bus line and the common electrode of IPS structure.

It is reported that low dielectric organic passivation films are a candidate to reduce crosstalk due to the manufacturing cost of the same thickness of an inorganic layer. A major effort for reducing the crosstalk of the IPS mode TFT-LCD is to optimize the electrode configuration to shield the pixel electrodes and the display area from the varying data-line voltages.

As a result, the IPS mode is more sensitive to process variations than the LC itself. Variations in array process, electrode width, height and surface topology must be accurately considered. Consequently, the optimum thickness of the organic layer or inorganic insulator layer are very important to consider for cost and performance optimization.

In this article CLEVER shows good agreement with measurement for TFT-LCD pixel structure and a capability to study crosstalk of IPS-mode TFT-LCDs.

## CLEVER for Flat-Pannel Display

CLEVER is successful in extracting parasitics even at very deep-submicron. CLEVER considers the aspect ratio which is the mesh quality of the active rand pixel region. Gate metal pattern with angle and undercut can also be simulated. The shape of the metal and film topology can be accurately simulated in using advanced CLEVER 3D process simulation and indispensable to predict accurate IPS TFT-LCD parasitic capacitance and crosstalk. Table 1 shows good agreement with measurement of different common-pixel electrode structures. Figure 1 is conventional IPS-mode electrode configuration for comparison.(ref 5)

| | meas(total)(fF) | Clever(Clc/Cdc/Clc+Cdc) | | |
|---|---|---|---|---|
| Ref | 99.6 | 51.0 | 53.4 | 104.4 |
| 1 | 93.46 | 41.2 | 52.6 | 93.8 |
| 2 | 91.25 | 36.5 | 54.3 | 90.8 |

Table 1. Common-Pixel & Common-Data Capacitance with different Common-Pixel Electrode Spacing (accuracy=5%)

*liquid crystal permittivity = 12.1

Ref/1/2: Pixel-Common space is increasing order.

## Coupling Capacitance Calculation of IPS Mode TFT-LCD Using CLEVER

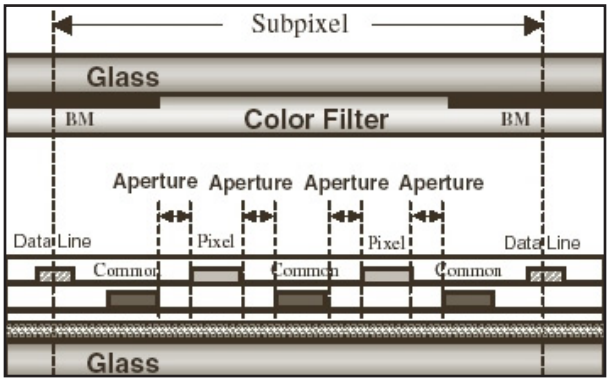


Figure 1. Conventional IPS mode TFT-LCD vertical structure(5).

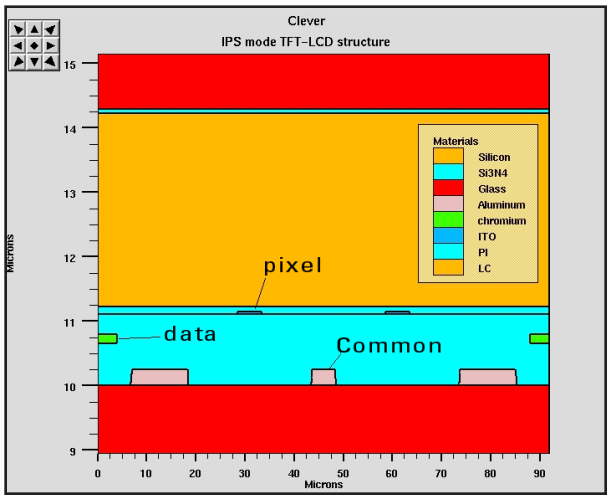


Figure 2. CLEVER structure. The tapered shape of common electrode is shown.

To prepare data for accurate capacitance extraction, simulated IPS mode electrode configuration using CLEVER is shown in Figure 2, where each electrode is simulated using advanced etch/depo process.

According to paper[1),(5)] coupling voltage of the pixel electrode dVp is defined as

$$\Delta V_p = \frac{C_{pd1}\Delta V_{d1} + C_{pd2}\Delta V_{d2}}{C_{LC} + C_{pd1} + C_{pd2} + C_{pg1} + C_{pg2} + C_{po} + C_{GS} + C_{st}} \quad (1)$$

Compared to TFT-TNs, the denominator of eq.(1) is small because all the electrodes are arranged on the same side of the substrate. Therefore in order to suppress Δ Vp on the IPS mode TFT-LCD, Cpd1 and Cpd2 have to be smaller than those of the TN mode TFT-LCD.

Capacitive coupling ratio CCR is a good approximation to represent the degree of crosstalk:

$$CCR = \frac{C_{pd1} + C_{pd2}}{C_{LC}(V) + C_{pd1} + C_{pd2} + C_{pg1} + C_{pg2} + C_{po} + C_{GS} + C_{st}} \quad (2)$$

Figure 3 shows electrodes configuration and an equivalent circuit described in equations (1) and (2).

$C_{lc}$ – liquid crystal capacitance

$C_{pd1}/C_{pd2}$ – coupling capacitance from the adjacent data line and the data-line to the pixel electrode.

$C_{pg1}/C_{pg2}$ – coupling capacitance from the adjacent gate line and gate line to pixel electrode.

$C_{po}$ – coupling capacitance from the pixel to common electrode in the array substrate.

$C_{gs}$ – TFT gat-to-source parasitic overlap capacitance.

$C_{st}$ – storage capacitance

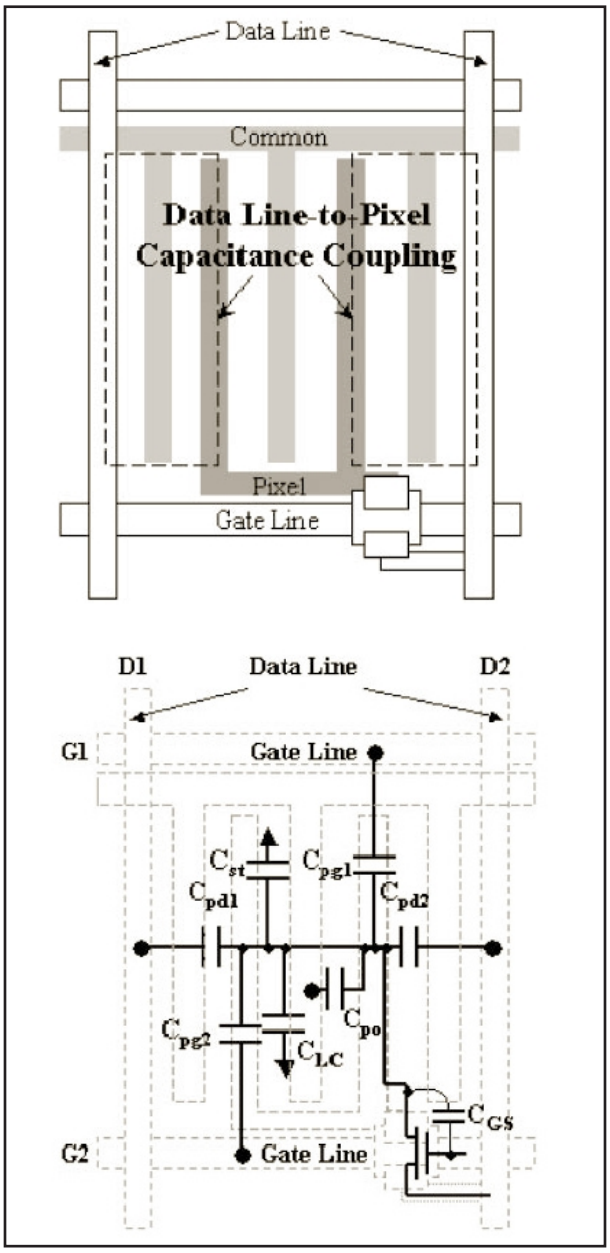


Figure 3. Equivalent circuit of a pixel.

Regarding voltage dependent Clc, constant permittivity of LC material can be considered when constant field is applied.

For comparison, Figure 4 shows simulated data-pixel and data-common electrode capacitance coupling which is extracted from two different kinds of pixel-common electrode configuration with oxide and inorganic layer(4).

Here, data-pixel capacitance and data-common capacitance of IPS structure was simulated using CLEVER(4).

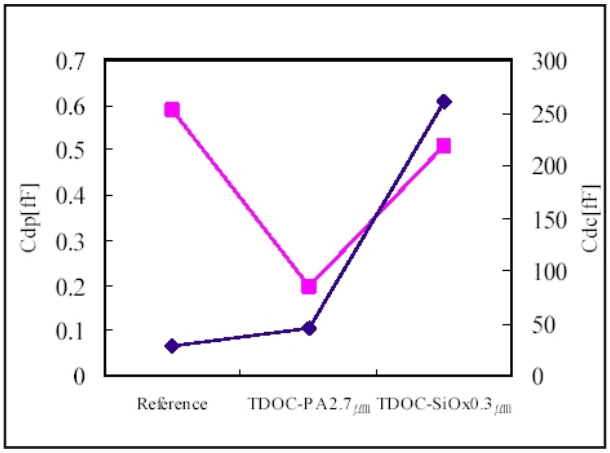


Figure 4. Simulated coupling capacitances of IPS structure with different electrode configuration(4) using CLEVER.

## RC Delay Simulation

From extracted parasitics netlist, the RC delay effect across data line can be simulated using SmartSpice. Only one pixel was simulated in this experiment.

```
M1 drain gate ito  nTFT w=49u l=38.5714u As=1274p
Ad=2439p Ps=150u Pd=610u Nrs=0.142857 Nrd=0 geo=0
C1   substrate gate   7.0162449e-14
C2   substrate drain  1.815544e-14
C3   substrate data   2.0479665e-14
C4   substrate ito    1.4275399e-13
C5   gate   drain  1.169502e-13
C6   gate   data   4.7088442e-14
C7   gate   ito    4.6344247e-13
C8   drain  ito    4.1971866e-15
C9   data   ito    7.8982418e-15
lib “tft.lib” ntft
vg gate 0 dc 20 pulse 0 20 0 1u 1u 108u 2m
vd drain 0 dc 10 pulse 0 10 0 1u 1u 2m 4m
vcom com 0 dc 5
mntft drain gate ito ntft w=20u l=5u
cst ito com 1.06p
re ito co 1.28k
c0 co lc 317f
rlc lc com 10g
clc lc com 125f
cgs gate ito 20f
cgd gate drain 20f
.tran 0.1u 8m
.save v(drain) v(gate) v(ito)
.end
```

Figure 5. Example of SPICE input file for a pixel simulation.

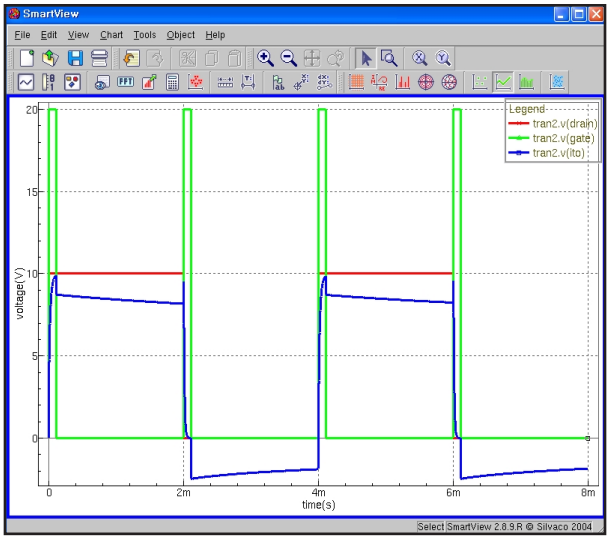


Figure 6. SmartSpice simulation of a pixel.

## Conclusion

Accurate 3D field solver in CLEVER can be applied to TFT-LCD design to predict origins of various coupling capacitances and so crosstalk.

The process variation such as passivation layer and the configuration of electrodes is easily simulated with CLEVER. From the integrated tool flow point of view, CLEVER-SmartSpice provide good framework for future full-panel designs.

## Acknowledgement

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## Appendix

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