# Understanding the AccuCore Work Flow and Processing Options

## Introduction

This application note is intended to help AccuCore users better understand the AccuCore work flow and the various processing options and methods available to address specific timing characterization and analysis needs. Readers are encouraged to review additional details in application note “Understanding AccuCore Timing Models and Their Uses”, the AccuCore Command Reference Manual, AccuCore Users Manual, AccuCore STA Reference Manual and AccuCore STA Users Manual.

## AccuCore Work Flow

AccuCore’s work flow is comprised of two main phases. Characterization and STA (Static Timing Analysis). AccuCore has many possible roles that it can play in support of a general chip design and verification work flow. Its main use, however, is dealing with custom digital blocks. Supported design styles include, but are not limited to, CMOS/SOI standard cells, static and dynamic logic circuits, passgate logic, footed and footless domino logic and many other transistor level styles. AccuCore generates functional and timing models of a block from a transistor level SPICE netlist either with or without parasitic RCs from either a hierarchical or flat netlist. Timing model generation can take two basic forms. One is the generation of a “top-level” block-oriented timing model for use as part of a full-chip timing planning or verification process. The other is the generation of an internal block timing model.

## Internal Timing Models

TThe internal block timing model can take several forms. The two root forms are “all-path” models or “path-specific” modeling. The choice of the two root forms is determined during the characterization phase. The main purpose of path-specific modeling is to bypass characterization of paths or section of logic that are not to be part of the final timing modeling or analysis thereby speeding up the process. This obviously requires detailed prior knowledge of the expected results and conditions and constitutes only a limited check. A condition limited analysis is also possible in the all-path form as a reduced set of boundary conditions.

## Characterization Phase

TThe characterization process results in a library of cell-level timing models with specific and unique characteristics as a result of the “in-place” SPICE characterization process of the blocks internal structure that is typically unique for each instance of a cell. The input netlist is partitioned into cell-level form by either automatic or user directed processing. In addition to the cell-level timing models, a structural verilog netlist and optional cell-level verilog functional models are output along with several other report and supplemental files to permit various post-processing and analyses.

The cell-level timing models typically generated are instance unique cell-level models based on the “in-place” SPICE characterization of a transistor-level netlist and any public SPICE models with optional RCs including coupling caps and exact slope and load conditions including “active-loads” for all internal nets. Results are nearly equivalent to that which results from a direct and complete block SPICE simulation. Simucad’s SmartSpice SPICE simulation engine is included and embedded in AccuCore and utilizes a high-speed proprietary API communication link to speed simulation. Third-party SPICE simulators are also supported, but largely unnecessary and significantly (typ 5-10x) slower resulting in longer run-times for equivalent accuracy levels. Both HSPICE, and Spectre netlist and SPICE model formats are 100% supported. Eldo SPICE models are also supported. No interpolation or table estimation are involved in the final sign-off timing characterization or analysis processes. Additionally no input vectors are required. Characterization is still a completely vector driven process for maximum accuracy including support for simultaneous Multiple Inputs Switching (MIS) effects, with required vectors determined automatically. Characterization takes place

in an ordered sequential fashion with the output of the prior cells driving the next cells inputs in a piecewise simulation process. This significantly speeds up the overall block characterization process which is an NP complete problem otherwise requiring an exponential quantity of vectors to fully cover all possible conditions and combinations. Statistical and heuristic methods could be used, but are not for maximum accuracy.

## "Cell-Level" vs. "Cell-Based"

Because of the unique method utilized, even though the final result of characterization is a library of cell-level timing models it is by no means a cell-based characterization process in the standard processing mode. AccuCore does offer a FAST_MODE method that is typically 50-100x faster than the standard method that is cell-based, but it is subject to the same fundamental accuracy limitations of traditional cell library characterization methods. This method is best utilized for non sign-off level timing analysis, generating SPICE path export netlists for sign-off simulation or pre-layout block-level timing models.

## Path-Specific Processing

With path-specific characterization modeling is incomplete and largely user directed with a specific intended use in mind. Uses can range from clocktree only analysis, blackbox block modeling, known worst-case path characterization and timing analysis, etc. AccuCore also supports internal to the block under characterization the use of blackbox models or declarations for sections of the design that are either incomplete, not digital logic (i.e. analog in nature), to be characterized later, previously or externally characterized or to be ignored for the purposes of the analysis. Desired timing paths can still be processed that pass through such sections with additional specified details during either the characterization and/or STA phases.

## STA Phase

DDuring the STA phase, AccuCore STA can generate the various block level timing models in varying degrees of complexity, focus points and formats. Options include blackbox, interface, interface-ring and compressed in Liberty .lib and SDF formats. Support is provided for incorporating optional DSPF RC parasitic backannotation info and/or Liberty .lib or SDF data on input. This is intended to cover the case where gate-level RC info was NOT utilized or available in the netlist for inter-cell parasitics during the characterization phase. Additionally, SPICE path and clocktree netlist export options exist. The decks generated by these processes include all stimulus and required timing measurements to validate or update the final timing effects. These exported simulation decks can be edited by the user to include any additional desired details or reporting prior to being run in a standard stand-alone SPICE simulator such as SmartSpice. The advantage of utilizing SmartSpice for such simulations is due to its built-in RC reduction processing options and extreme high-capacity and dedicated RC netlist handling capabilities and solvers and is a "true" SPICE simulation engine.

## Conclusion

AccuCore is a powerful and flexible tool for the characterization and analysis of complex block level digital logic circuits. Outlined above is an overview of typical work flows and a number of processing options available to users. Additional options and details exist, but are too numerous to detail in this ap note. For additional info the reader is encouraged to review the additional references discussed in the introduction section of this application note. Additional material and training is available by contacting your local Sales Account Manager. Simucad Token-Based users have access to AccuCore and other tools without the need for an additional license. See your Sales Account Manager for additional details and requirements or to request an evaluation license.