How to Define Optimal Slopes & Loads for Cell Characterization

Introduction

This application note is intended to help guide AccuCell users towards an optimal custom solution. AccuCell users have complete control over what and how to (re-) characterize cell libraries.

Re-Characterization

If you are performing re-characterization, extended or alternate operating point characterization then the issue can be largely avoided. Use of the same points and table sizes presently in use or that match parts of the library that are not being changed is a solution that typically yields adequate results. No other options need be considered in most cases.

Optimized Slopes

For initial or customized characterization, however, defining optimal slopes is less straight forward than optimal loads. The slope task can be split in to two parts.

1) Definition of the upper and lower index limits

2) Definition of the distribution of the remaining table points.

The relevant questions are:

How many table points are needed? What is adequate? What is the impact of specifying too many? Or too little? The upper index value is normally the max_transition value. The proper max_transition value depends on the max_capacitance value and vice-versa.

If time permits addition research, if a reference library is unavailable or if performing other than re-characterization for alternate corner conditions then checking some or all of the assumptions or givens against expected operational limits and level of accuracy requirements is warranted.

Alternatives

If requirements are uncertain, and the best possible accuracy is required then cell-based characterization and static timing analysis may not be the right solution. Consider AccuCore with its transistor-level SPICE-driven path-based block characterization and static timing analysis.

Cell-Based

Cell-based characterization has several fundamental limitations inherent with the methodology. Whether or not it is NLDM, CCS, ESCM or any other “cell-based” method. If timing results of <50ps for long, deep, logic paths is required then do not use cell-based timing analysis methods. No matter how accurate the timing engine is the characterization cannot be performed at a cell-level with the required level of accuracy. Cell input sensitivity to input waveform stimulus variations prohibit it. An error of 1-2% of SPICE over a timing path that is 2500-5000ps long (i.e. 2.5-5.0ns or 200-400MHZ clock period) is significant. For a logic depth of 20 this equates to a path timing budget of 125-250ps per stage and 1-2% of that is 1.25ps-5ps assuming zero timing analysis error. Even if simulations are run at 0.1ps time step during transient analysis, stimulus waveform limitations cannot be overcome, since the resulting variation due cell drive characteristics vs load and RC configuration yields different timing behavior greater than this.

Accuracy

If a cell-based method with relaxed accuracy and no RC loading extremes or excessive slopes is used, (i.e. only what is needed to create a netlist from logic synthesis and converge timing in place-n-route) and “sign-off” quality timing is not required then the answer is about 5-10%.

To ensure that ALL cell characterization results meet that accuracy limit, a specific number of points for slopes and loads are required at specific values. One way to deter-

mine this is to let AccuCell's Automatic Table Selection (ATS) algorithms calculate this. The number of timing templates is not a significant restriction in library creation for most timing analysis engines therefore each cell (or drive strength) can have its own set of values.

Loads can be varied, but the slopes need to all fit within the same general range. To limit noise delay from being a significant potential component of path timing, keep edges moderately fast so "propagation delay" (i.e. the part doing real computational work) is about equal to transition delay from driving the parasitic wire load.

Max_transition

As a general rule, a good upper limit for the clocks (and the data to some extent) is a 10-90 edge rate of ~ 10-15% of the clock period. Assuming (for the moment) 200-400MHz clocks (i.e. 2500-5000ps) this is about 250-750ps 10-90 edge rate for the clocks and about double that worst-case for the data. This range is required to cover the worst part of the timing path conditions. In STA the 50% point is the typical switching threshold yielding a max 10-50% time (for the data) of ~750ps. To minimize waveform error effects characterize for 30-70 instead of 10-90. The resultant transition delay slope index upper limit (i.e max_transition) is ~750ps.

Max_capacitance

From max_transition, individually determine for each cell max_capacitance. This is the capacitance that results in max_transition on the output when max_transition is used on input.

Lower Limits

The worst case for a lower index slope is the fastest possible edge that a pull-down of max strength driving a single min size inverter with no wireload can generate. The pin capacitance of a min size inverter is usually the lower capacitance index.

However, this is typically not faster than 10% of the typical gate delay, so if a gate delay is ~25ps then the lower limit would be 2.5ps. This is a very pessimistically low (fast) value. Approx half (50%) of a gate delay is a more reasonable value. In non-VDSM technology where gate delays are upwards of 10x this value the min transition would be pro-rata higher.

Use of a FO=1 of the gate driving itself is another common, and more realistic, min transition value. The same indexes are used for both rise and fall.

Delay curves tend to be very linear with the full range of loading conditions at fast slew rates and gradually become highly non-linear at light loading curves as edge rates slow down.

Library Differences

For a slow/worstcase library the min transition is important for maximum performance circuit timing, setting min transition higher results in a conservative timing result. This behavior, however, for a fast/best case library is exactly opposite of what is desired. As such some libraries sometimes are generated with min transition = "0" for the lowest index. This is not physically possible, but guarantees a definite lower bound for delay.

Delay/slope values for a "0" entry can either be calculated via intercept-method as a post process procedure or approximated by an input edge and .tran time step = at most 10% of the gate delay or ~1ps. As a result characterization slows down proportionately. Dynamic time step control in the SPICE simulation will dynamically alter this value up or down by a factor of up to 10x to help speed simulation without direct SPICE option restriction.

Thresholds

Define the slopes according to the time between thresholds and not VDD VSS ramp timing if/when in the default mode of EXTEND_SLOPE 1 (in AccuCell) and as ramp times if/when EXTEND_SLOPE 0.

Example

NOTE: Some prefer the same 2^N method (as typ used for loads) for slopes which is based on the notion of bandwidth tracking, others prefer a straight linear distribution between the upper and lower limits or other similar method. Skipping over details and without explaining why for the moment assume the following:

Common slope indexes for a library with an ~25ps gate delay and 70/30 thresholds:

SS = 0.01 0.1 0.2 0.3 0.4 0.5 0.6

FF = 0.001 0.01 0.02 0.04 0.08 0.16 0.32

translates to RAMP times of 1/(0.7-0.3)=(1/0.4)=2.5x:

SS = 0.025 0.25 0.5 0.75 1.0 1.25 1.5

FF = 0.0025 0.025 0.05 0.1 0.2 0.4 0.8

Why?

NOTE: A 25ps gate delay is based on a 50% transition with the assumption that the second half of the transition completes in double of the first halh. At light loading this is true, but at heavy loading it many only complete in triple this time due to RC e^x or ln(x) effect.

The example slope range permits accurate timing of gate stage delays down to a 72:1 ratio (i.e. 1.8ns vs 25ps). This roughly equates to 64 equivalent loads. 3-4 equivalent loads is a common circuit fan-out load, as this is the load that results in optimal path timing. Use of a 10:1 ratio for the first slope step yields good slope range and a reasonable distribution across the majority of the slopes while keeping the error minimized. Timing is fairly linear for the lower slope range. Use of a linear distribution for the slow/worst case corner emphasizes the number of slope points in the non-linear range where a worst case library is most likely to see the majority of it timing analysis use. Use of a 2^N distribution for the fast/best case library emphasizes the number of slope points in the region where the highest relative delay error occurs and would have the greatest impact on fast circuit path analysis. Slow corner to fast corner timing ratio is typically on the order of 2:1 hence the ~2:1 ratio in max_transition between these corners.

Good Values

The purpose of the index values is to minimize the interpolation error for a given cell. Each cell can have different index values. Also, cells of the same drive strength use the same load index values and all cells usually use the same slope values. At or near MAXCAP the delay is very linear with load unless taken to an extreme. At very light loads delay is very non-linear. (i.e. largest rate of delay change per unit change in load from one load to the next and “curvature” is at a max).

Relative delay error is as important as absolute delay error since the actual clock operation speed is not known in general. Using a square-law distribution tends to be a good trade-off of all factors assuming a reasonable, but minimal, number of points in the table. Run times and memory use are a factor in synthesis and static timing tools so use of many large tables in large cell sets slows things down, but not a whole lot and accuracy is a primary goal. Check with your synthesis vendor for details on their possible limitations and difficulties in dealing with unique table per cell type libraries and large table sizes.

An inverter is usually, but not always, the limiting case for table index values and interpolation error. AccuCell’s ASIC mode understands this and is why this cell type is used as the reference cell in determining the index values for all other cells in the same category (i.e. drive strength).

AccuCell’s MAXCAP is usually limited by MAXSLOPE. MAXSLOPE is usually limited by either the cell technology and/or application clock speed. Minimum chip power is typically attained at fast to moderate edge rates. Slow edges in general are bad for many reasons. Noise induced delay variation is the primary reason, time model accuracy is another, and power is typically the last. This assumes that the application clock speed doesn’t limit it first.

Conclusion

AccuCell has many powerful features and great flexibility to allow users to implement cell characterization per a custom specification or to perform most of the work automatically that together with this application note enables accurate cell library characterization to be performed.