Automatic Port Determination in Catalyst

Introduction

A new Tcl feature has been added in Catalyst for automatically determining most ports of a block without any prior knowledge of the block. Suggested INPUTS, OUTPUTS, POWERS & GROUNDS will be reported after analysis of the block SPICE netlist. Clocks will be included as INPUTS reported, but will NOT categorized as clocks. Bi-directional INOUTS ports (driven by tri-states) are NOT presently supported. Additionally, ports connected to pass-gates are also NOT presently supported. If your block contains ports of this nature they will need to be manually specified.

Purpose

The purpose of this feature is to aid in the creation of the definition of ports of a block when such details are NOT readily available. To convert the reported data into a Catalyst .cfg file for SPICE-to-Verilog conversion, simply list the nets as reported for the appropriate declarations. For Clocks, once these have been determined from the possible list of ALL inputs, simply declare each clock with its own domain in a separate CLOCKS statement. Clocks with the SAME synchronization phase and common time base can be listed together. Clocks with opposite phase should be declared with the SAME domain name but proceeded with a "!"(bang).

Syntax:

```
analyze_boundary <config_file>
```

The initial .cfg file needs only two commands defined and supports the optional inclusion of a third. Order of the commands does NOT matter.

```
IN_FILE_NAME my_block.sp
MOSFET_TYPE <device_type_name> {pmos|nmos}
[SPICE_TOP_SUBCKT <top_level_subckt_name>]
```

IN_FILE_NAME – Specifies the file name of the SPICE netlist to analyze. The circuit may be split across multiple files. A list of file names may specified or the command may be specified multiple times to refer to multiple files.

MOSFET_TYPE – Specifies an active switch device type and its polarity type. This command must be called multiple times to individually define each and every active switching device type that exists in the netlist.

SPICE_TOP_SUBCKT – Specifies an optional .SUBCKT name of the top-level entity defined in the netlist. This entity need not be called in the netlist file only defined. This top-level .SUBCKT may contain additional embedded .SUBCKTs and/or Xcalls referencing other hierarchical instances.

Example:

(in the <block_name>.tcl file)

```
analyze_boundary my_block_init.cfg
```

(in the <block_name>.cfg file)

```
IN_FILE_NAME my_lock.sp
MOSFET_TYPE pch pmos
MOSFET_TYPE nch nmos
SPICE_TOP_SUBCKT top
```

(in the log file is reported)

```
INPUTS a b c clk
OUTPUTS out
POWERS vdd
GROUNDS gnd
```

NOTE: global power and ground nets will be reported "locally" as x1-vdd x2-vdd x1-gnd x2-gnd etc. They should be declared by their global name instead of the local reference in the .cfg file.

(in the <block_name>.cfg file ADD)

```
INPUTS a b c
CLOCKS foo clk
OUTPUTS out
POWERS vdd
GROUNDS gnd
```

Where “foo” is an arbitrary clock domain name.

Appendix

The follow outlines the basic syntax of the port commands in a .cfg file.

Syntax:

```
INPUTS <inputs>
CLOCKS [!]<domain_name> <clocks>
OUTPUTS <outputs>
INOUTS <bi-dirs>
POWERS <powers>
GROUNDS <grounds>
```