SmartSpice SEU Module

Introduction

Information in electronic circuits is stored and communicated as a collection of electric charges. Any event which upsets the stored or communicated charge can cause errors in the circuit output. These errors are called transient faults, soft errors (SE) or single event upsets (SEU). The event causing the upset can be an energetic nuclear particle or an electrical source.

The nuclear particles which create these upsetting events are either cosmic rays which bombard the earth constantly from space or radioactive atoms which exist in trace amounts in all materials due to atomic decay. Atmospheric nuclear particles include alpha- particles, protons and neutrons. Electrical sources are power supply noise, electromagnetic interference (EMI) or radiation from lightning. Memories are considered most vulnerable to transients due to their spatial density and the amount of information they store. As technology continues to scale in the nanometer era, it is important to consider memory arrays and core logic when estimating microprocessor soft error rate. Single Event Transients (SETs) occur when an energetic particle strikes a combinational logic element. The charge deposited by the particle causes a transient voltage disturbance, which can propagate to a storage element and be latched, resulting in Single Event Upset (SEU). The logic design style, storage element behavior, and system timing requirements greatly impact the probability that an SET will cause an SEU. These effects are explored through circuit simulations and heavyion testing of prototype devices. Soft errors present a real challenge for high performance and low-power microprocessor design.

The Messenger Current Modeling

By default SmartSpice SEE capability uses Messenger's fault model [1] to account for soft errors in the circuit due to the impact of incident particles. To have an accurate result it is important to localize the effect inside the transistor and not with an outside macro-model. In SmartSpice a current generator is inserted in the intrinsic nodes of the transistors (BSIM3, Gummel-Poon, MEXTRAM, BSIMSOI, VBIC, Quasi-RC, and EKV). The shape of the generated current is closely approximated by double-exponential source available in SmartSpice. SmartSpice also allows user defined SE models through a PWL and EXP source functions, SmartSpice's behavioral A device and through Verilog-A. Messenger's fault model is a double-exponential current source.

The Theoretical expression is the following :

$$i(t) = I_{SEU} \cdot (\exp(-t/\tau_F) - \exp(-t/\tau_R))$$

- ISEU depends on the amount of injected charge and may be positive or negative.
- f represents the collection time-constant of the junction.
- r represents the ion-track establishment time constant.

The expression above (Equation) can also be expressed using the deposited charge dependence:

$$i(t) = \frac{Q_{dep}}{\tau_F - \tau_R} \cdot (\exp(-t/\tau_F) - \exp(-t/\tau_R))$$

- Qdep = ((q*ρ*Lf *LET)/Ee,h))
  - q= electron charge(1.6E-19C)
  - ρ =material density(2.33g/cm3) for silicon
  - Lf= Funnel Length (cm)
  - LET=Linear Energy Transfer (MeV • cm^2 / mg)
  - Ee,h = Energy rrequired to create e-h pair (3.6eV in Si)

Innovative Features

SmartSpice SEU part is based on Messenger Current Modeling. To have an accurate result it is important to localize the effect inside the transistor and not with an

outside macro-model. In SmartSpice it is included in the intrinsic nodes of the transistors. The user also have the possibility to implement his own intrinsic model.

A complete SEU analyze needs more option to have the possibility to represent realistically the impact. First of all, multiple impacts must be simulated in the same time or nearly in the same time: two separated impacts may not produce an error in a circuit, but the two same cumulated impacts may change the state of a cell.

Then we must find some criteria to say if there is an upset or not. An impact may shortly change the state of a transistor. But if the circuit is robust enough, it will return in its original state and in this condition we cannot say that there is an upset. The best way is probably to have some user defined parameters, that allow parameterizing it. SmartSpice SEU offers two possibilities: it allows defining an absolute or relative error in a given time. In other words, if after a fixed time the voltage of the node does not meet the tolerance entered by the user, the simulator outputs an upset.

Finally, we have the possibility to check an upset anywhere in the cell. Some cells have redundancy integrated to avoid output change. So it may be possible that locally there is an upset, but this upset is not critical if it does not change the global behavior of the cell. It is sometimes necessary to watch other nodes than the one impacted. If there is no upset on these nodes (output nodes…), the cell is considered as safe.

We can also consider the problem in an other way: what would be the maximum LET (Linear Energy Transfer) before obtaining an upset? It is possible to answer this question with the QCRIT feature of SmartSpice: it automatically runs in batch several simulation to directly gives the value of the LET to obtain the upset.

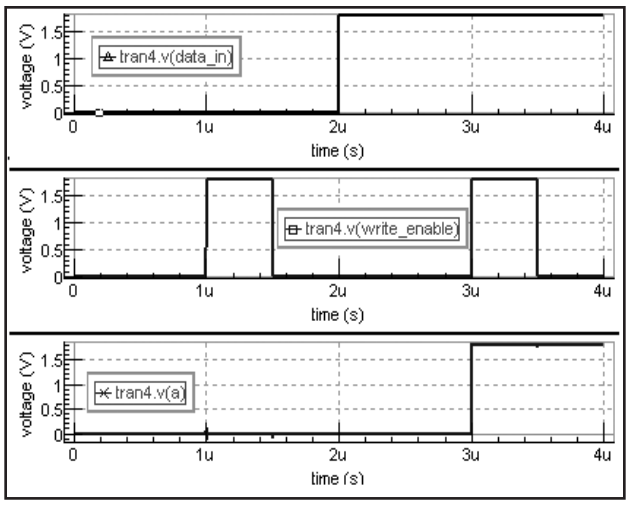

Figure 2. Two Write Cycles.

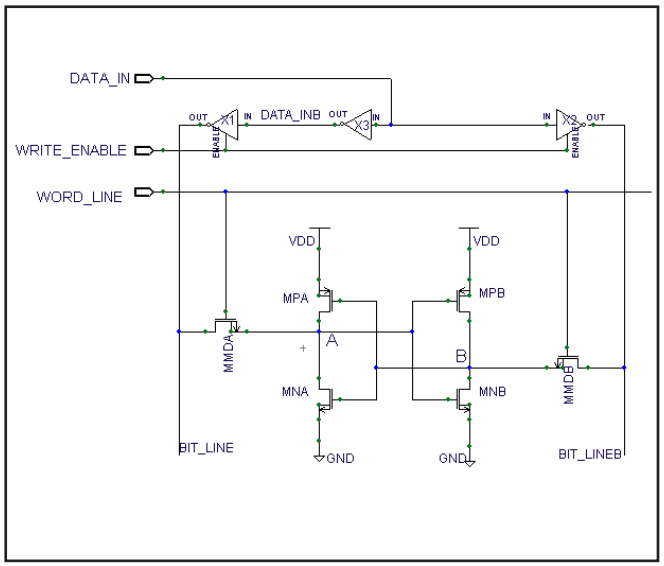

Figure 1. 6Mos Sram.

Example

We now consider a 6 Mos sram with the Data_in, Write_enable and Word_line input signals (Figure 1).

A non perturbated simulation gives the following result (Figure 2): The V(write_enable) signal write a “0” at 1us and write a “1” at 3us. V(a) corresponding to the stored information is correct.

If we add a perturbation in the MPA drain MOS (Fig 1) at

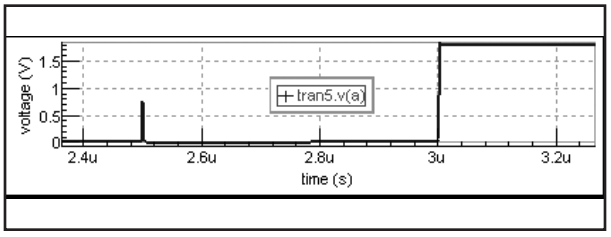

Figure 3. SEU impact a 2.5us (LET=5).

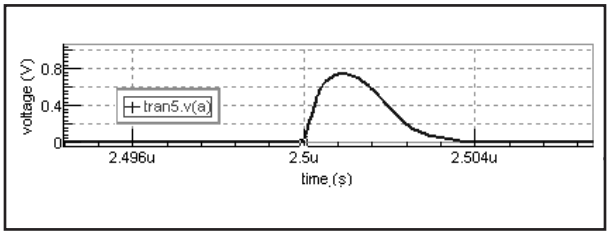

Figure 4. SEU impact at 2.5us (LET=5): Zoom.

2.5us with a ".rad" analysis from SmartSpice we obtain the result in Figure 3.

```
.RAD SEE=1
   + DEVICE=MPA
   + START = 2.5u
   + TAUR =0.05n TAUF =0.7n LF=1u
   + LET=5
```

A glitch appears in V(a). A zoom at 2.5us gives the Figure 4.

We clearly see the influence of the impact but in this situation it does not involve any upset. V(a) stills correct. We now increase the LET to 6 and we obtain the Figure 5.

The Energy is enough to produce a non wishing state in the memory cell. At time t=2.5us the data stored switch from "0" to "1".

The last figure (Figure 6) shows 2 impacts separated from 3ns with a LET of 5. One on the MOS MPA, an other one on MNA. Both influences are cumulated.

```
.RAD SEE=2
   + DEVICE=MPA MNA
   + START = 2.500u 2.503u
   + TAUR =0.05n 0.05n
   +TAUF =0.7n 0.7n
   + LF=1u LF=1u
   + LET=5 LET=5
```

We can see that this circuit is robust enough to avoid an upset.

Reference

[1] G. Messenger, M. Milton, "Single Event Phenomena", Chapman & Hall editor, 1997.

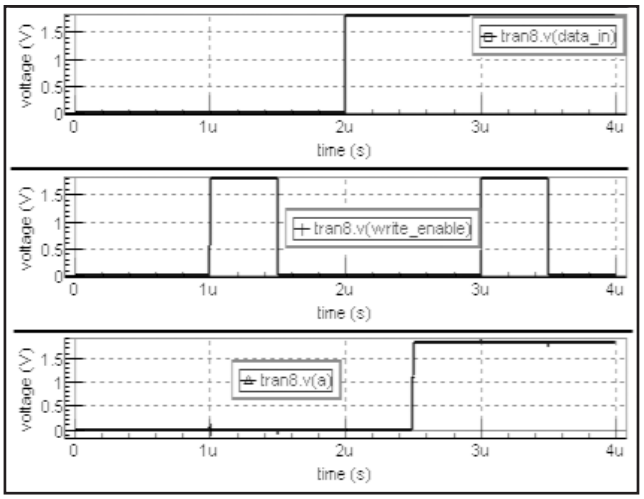

Figure 5. SEU at 2.5us with an upset.

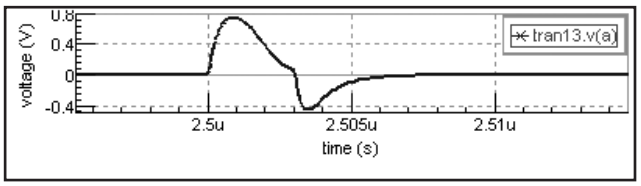

Figure 6. Two impacts separated from 3ns.