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A Semi-Analytical Model for the Subthreshold Behavior of FinFLASH Structures

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Abstract—In this paper we present an original semi-analytical model for the subthreshold electrical behavior of complex 3D structures as the SOI FinFLASH devices. This physically-based model, which does not need any fitting parameter, solves the Poisson equation for a fin covered by trapped charges in the active dielectrics. The analytical results are compared with fully 3D numerical simulations and a good agreement is obtained down to fins with very small feature sizes (order of tens of nm). This model can be efficiently used to gain information on important cell electrical behaviors as the threshold voltage shift ΔVth and the subthreshold slope factor S.

I. Introduction

The FinFLASH device in trigate (W ≈ H, see Fig. 1) or double-gate (H _ W) configuration is currently investigated as one of the most promising solutions to replace conventional planar FLASH structures beyond the 32 nm technology node[1]-[2]. The main advantages of the FinFLASH device are its compact layout, moreover fully compatible with future generations of multi-gate CMOS, and its excellent electrical performance due to the enhanced coupling between the gate and the active channel. In this frame, it is today of utmost importance to provide a simple approach which allows us to describe the most important electrical parameters of the memory operation without applying time consuming 3D numerical simulations.

In this paper we present 3D fully numerical simulations of FinFLASH devices (Fig. 2a) to substantiate our simpler analytical approach for the comprehension of the electrical behavior of such complex structures (see Fig. 2b). The comparison will be focused on the subthreshold electrostatics (Fig. 3) as well as on the electron transport (see Fig. 4 and Fig. 5). In the end we will analyze the limit of validity of our model in terms of doping level (see Fig. 7) and minimum feature sizes of the fin.

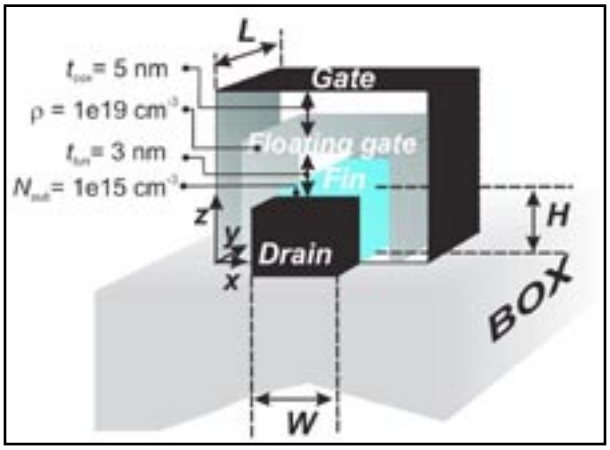

Fig 1. Plot of the modeled SOI FinFLASH structure. Relevant features used both in the model and in 3D TCAD simulations are highlighted.

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INSIDE

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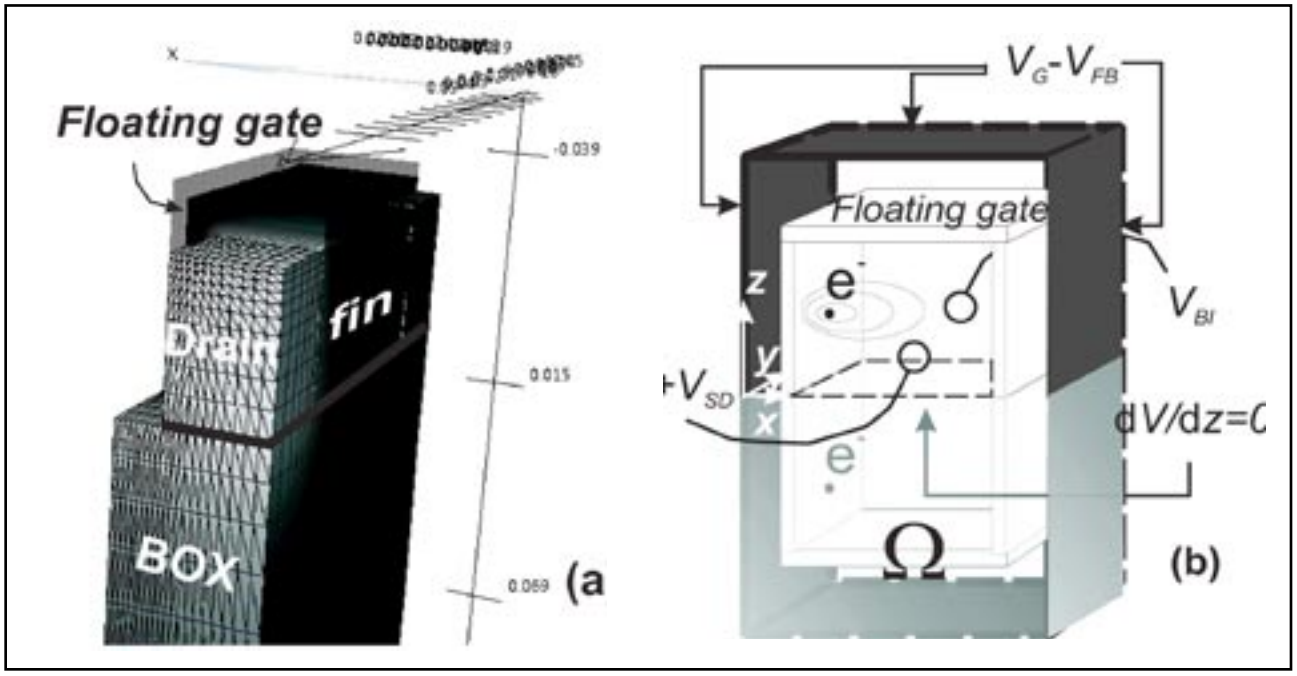

Fig. 2. (a) FinFLASH structure employed in 3D simulations. Only half a structure is represented and simulated because of symmetry considerations with respect to a longitudinal plane at the middle of the device. The gate stack is transparent to let appear the floating gate around the fin. (b) FinFLASH schematic employed for the analytical model to solve the electrostatics under weak inversion. Among the boundary conditions, it should be noted the Neumann condition (dV/dz = 0) at the bottom side due to the presence of the thick BOX. Source and drain equivalent metallic plates are transparent to let appear the domain of analysis. The point charges are afterwards integrated to obtain the uniformly charged floating gate.

II. Model for Electrostatics and Transport

The bases of the physics of our model are herewith detailed. *The model solves the potential of a FinFLASH device, Ψ_{FFLASH}, as the sum of the potential of a FinFET fresh device, Ψ_{ZFFET}, plus the potential due to the trapped charges around the fin* $\Psi_{Zq\text{-}tot}$. The superposition principle can be used if the impact of mobile charges is neglected, therefore the device is operated in the subthreshold region.

The model starts from the solution of the Laplace equation for Ψ_{FFET} in the FinFET space domain Ω (see Fig. 2b) with mixed boundary condition on Γ [3]. Ψ_{FFET}, indeed, is the potential distribution of a non-doped fin where mobile charges are neglected and the control oxide region is considered as an equivalent silicon region with proper thickness, in order not to treat mathematically the Si/SiO_2 interface. The source and drain are treated as perfect metals. Thus Ψ_{FFET} solves the following Laplace problem:

$$\begin{cases} \Delta\Psi_{FFET} = 0 & \text{in } \Omega \\ \psi_{tg} = V_G - V_{FB} \quad \psi_{rg} = V_G - V_{FB} & \\ \psi_{lg} = V_G - V_{FB} \quad \psi_S = V_{bi} & \text{on } \Gamma \\ \psi_D = V_{bi} + V_{DS} \quad d\psi_{BOX}/dz = 0 & \end{cases} \tag{1}$$

where ψ_{rtg}, ψ_{rrg}, ψrlg are respectively the top, right and left gate potentials, ψ_{BOX} is the potential at the interface silicon/BOX, ψ_S and ψ_D are respectively the source and drain potentials (see Fig. 2b).

Then we treat separately the impact of a point trapped charge, Ψ_q. Thus Ψ_q solves the following Poisson problem:

$$\begin{cases} \Delta\Psi_q = -\frac{q}{\varepsilon_{si}}\delta(x-x_0)\delta(y-y_0)\delta(z-z_0) & \text{in } \Omega \\ \psi_{tg} = 0 \quad \psi_{rg} = 0 & \\ \psi_{lg} = 0 \quad \psi_S = 0 & \text{on } \Gamma \\ \psi_D = 0 \quad d\psi_{BOX}/dz = 0 & \end{cases} \tag{2}$$

where $\varepsilon_{si(/ox)}$ is the silicon(/oxide) permittivity, δ is a Dirac Delta function of the coordinates of the charge x_0, y_0, z_0. We originally used the *Green's function method* to find an analytical solution to the point charge potential £Zq in a 3D domain [4], where the mixed boundary conditions are properly considered. First the solution to the equivalent homogeneous Dirichlet problem of (2) imposes the research of a Green's function G, which solves the following:

$$\begin{cases} \Delta G = \delta(x-x_0)\delta(y-y_0)\delta(z-z_0) & \text{in } \Omega \\ G = 0 & \text{on } \Gamma \end{cases} \tag{3}$$

On the other hand, the Neumann condition at the BOX interface is obtained through the impostion of a fictitious charge of identical sign of the actual charge, mirrored with respect to the plane at z = 0 (look at Fig. 2b).

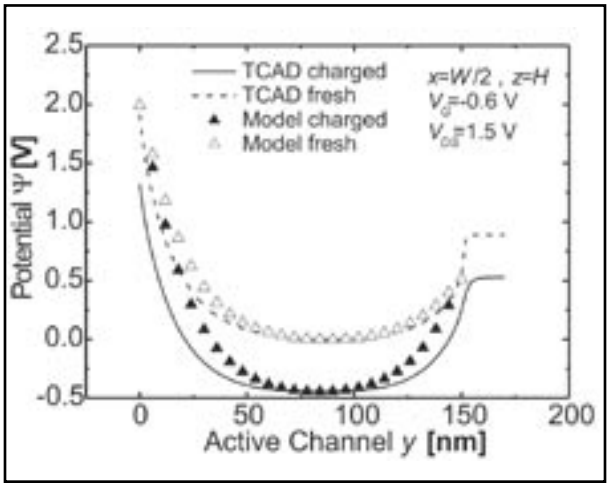

Fig. 3. Plot of the fin potential along a longitudinal cut for a fresh and charged device. A fine agreement between the TCAD and model results is apparent even for high drain-to-source voltage reading (W = 40 nm, H = 30 nm).

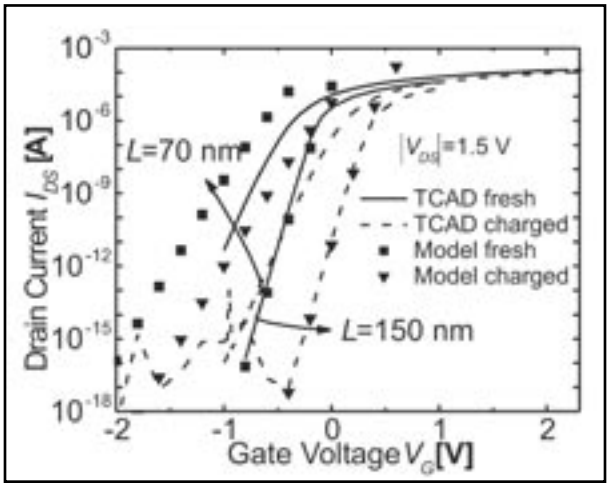

Fig. 4. Plot of the electron concentration along the fin height for a fresh and a charged device assuming n = ni exp(q£ZFFLASH/KT), (W = 40 nm, H = 30 nm).

Thus for a charge q located at (x_0, y_0, z_0), the potential Ψq in (x, y, z) is described by the following Fourier series:

$$\Psi_q = \frac{-1}{\epsilon_{si} L W_{eff} 2H_{eff}} \sum_{m,n,p}^{\infty} \frac{\sin\left(\frac{p\pi}{2}\right)\sin\left(\frac{m\pi x_0}{W_{eff}}\right)\sin\left(\frac{n\pi y_0}{L}\right)\cos\left(\frac{p\pi z_0}{2H_{eff}}\right)}{m^2/W_{eff}^2 + n^2/L^2 + p^2/4H_{eff}^2} \cdot \sin\left(\frac{m\pi x}{W_{eff}}\right)\sin\left(\frac{n\pi y}{L}\right)\cos\left(\frac{p\pi(z-H_{eff})}{2H_{eff}}\right), \quad (4)$$

where $W_{eff} = W + 2$ **X** $(t_{tun} + t_{cox} + t_{ch})$, $H_{eff} = H +$ **X** $(t_{tun} + t_{cox} + t_{ch})$ W and H are the width and height of the fin, while t_{tun}, t_{cox}, t_{ch} are the tunneling, control and trapping medium oxide thicknesses, as shown in Fig.1.

The impact of each point charge is afterwards integrated in the space domain to obtain the analytical solution for the potential of a *uniform distribution* of charges around the fin $\Psi_{Zq\text{-}tot}$.

Once the potential Ψ_{FFLASH} of the fin is known, the drain current is calculated through the numerical integration of the electron current density J along the dimensions of the fin, where we assumed a Boltzmann distribution for mobile charges and the Fermi energy level gradient negligible in the xz transversal plane. We obtain:

$$I_{DS} = -KT\mu n_i \frac{1 - \exp(-qV_{DS}/KT)}{\int_0^L \frac{dy}{\int_0^W dx \int_0^H dz \exp(q\Psi_{FFLASH}/KT)}}, \quad (5)$$

where K is the Boltzmann constant, T is the lattice temperature, μ is the average electron mobility, ni the intrinsic electron concentration and V_{DS} is the drain-to-source reading voltage.

III. Numerical Simulations and Discussion

In order to validate our approach, we compared the results obtained by means of the analytical model with a large set of 3D TCAD simulations[5] while varying the features of the memory cell (i.e. dimensions of the fin, tunnel and top oxide thicknesses, amount of trapped charge, etc.). In Fig. 3, we show a comparison of the potential along y for a fresh and a charged cell. We see that we obtain a good agreement between the numerical and the analytical model especially capturing the minimum of the potential, which is the energy barrier peak that has to be overcome by electrons travelling towards the drain. However we note some mismatch approaching the source and drain junction. The potential around these regions is overestimated because the drain and source

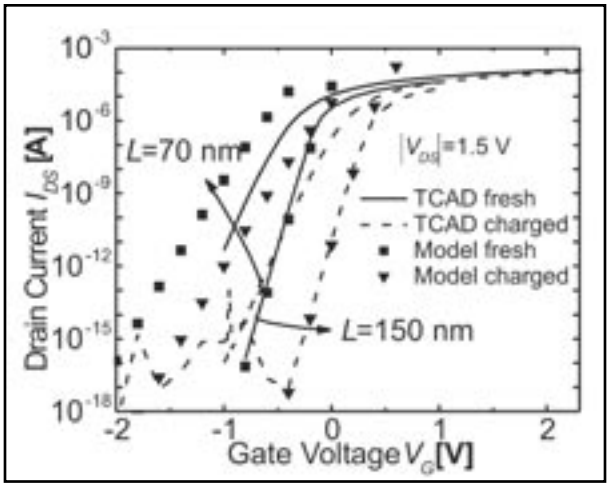

Fig. 5. Comparison between the transfer characteristics as obtained by TCAD and and by our model for a long and a short FinFLASH device (W = 40 nm, H = 30 nm). We see that for L = 70 nm the model looses accuracy in the Vth value, however still a fine ΔVth and S factor are provided.

are represented by metallic plates (see Fig. 2b) which enforce Dirichlet boundary conditions not only along the extremes of the silicon fin, but also along the sides of the oxides up to the gate, where we should have preferably a Neumann boundary condition. This approximation had to be done in order to obtain an analytical solution to our problem, and the limits of validity will be discussed in section IV.

In Fig. 4 we show a comparison of the electron concentration along z. Indeed, the efficiency of our model in describing both the electrostatics, based on (4), and the transport in 3D structures, based on (5), clearly appears.

In Fig. 5 we compare the transfer characteristics IDS-VG for two different devices with L = 150 nm and L = 70 nm, and we note that the model fairly agrees with the numerical simulations even for the scaled device.We highlight the fact that we are in the worst reading condition, as we used VDS = 1.5 V, concerning the reliability of the analytical model results.

In Fig.6 we extended the comparison of ΔVth and S, the slope factor, to devices with different fin lengths and different aspect ratios, in order to analyze the typical features of a FinFLASH in the double-gate configuration (Fig. 6a) or in a trigate configuration (Fig. 6b). We notice a good agreement in the overall electrical behaviors down to L = 50 - 100 nm.

IV. Limits of Validity

In this section we will analyze the limits of validity posed by the fin doping level and the Dirichlet boundary conditions at source/drain.

Our model is tailored for intrinsic fins, however due to the fact that the electrostatics in such structures is governed more by the geometry of the fin than by its doping level [6], we explored the validity of our approach for doped fins. In Fig. 7 we show the behavior of the programming window with respect to the fin doping level for small and large devices. Even if threshold voltages vary little with respect to fin doping (not shown in the figure), we see that the programming window remains quite constant, thus our model can be used to well predict the threshold voltage shift even for doped fully-depleted devices.

Concerning the Dirichlet boundary conditions at source and drain, we have to consider that in actual devices source and drain enforce a fixed voltage at the junction with the silicon fin and not over all the area up to the gate contact, as sketched in Fig. 2b. Moreover in the analytical model the oxide should be interpreted mathematically as an equivalent silicon region with suitable enlarged thickness, thus this problem put in serious challenge the model bases. This issue is even more serious for memory devices where the gate stack region is very thick with respect to fin sizes.

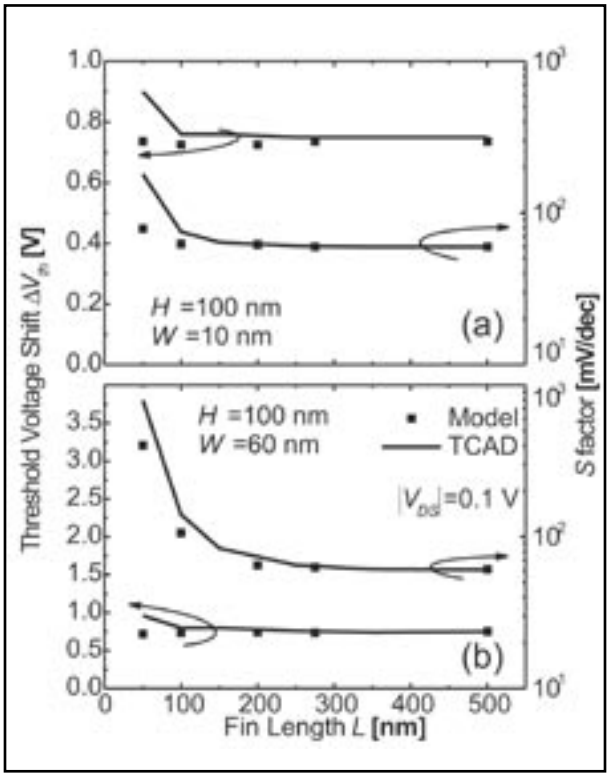

Fig. 6. Threshold voltage shift and slope factor for (a) a double-gate FinFLASH (H _ W)and for (b) a trigate FinFLASH (H ≈ W). We see that an excellent agreement is found down to L = 100 nm. Below this value the model suffers of excessive impact of drain and source voltages on channel potential.

As evidenced in Ref. [3], we can highlight a natural decay length L_d of influence of the drain voltage on the fin electrostatics:

$$L_d = \frac{1}{\pi\sqrt{\frac{1}{W_{eff}} + \frac{1}{2H_{eff}}}} \qquad (6)$$

This decay length has to be short (i.e. around a half) with respect to the distance between the drain junction and the location of the potential minimum, in order to be sure that the error of the perfect Dirichlet boundary condition at source/drain does not propagate on the drain current calculation. Indeed the minimum of the potential govern the subthreshold current [7], and for resonable value of the reading voltage VDS, it remains around the center of the device length. Therefore we can establish as a safe value for the minimum features of the memory device with thick gate stack, what we obtain from the following criterion:

$$L_d \leq L/4, \qquad (7)$$

which means, for instance, a device with features highlighted in Fig. 1 and W=40 nm, H=30 nm, L=90 nm.

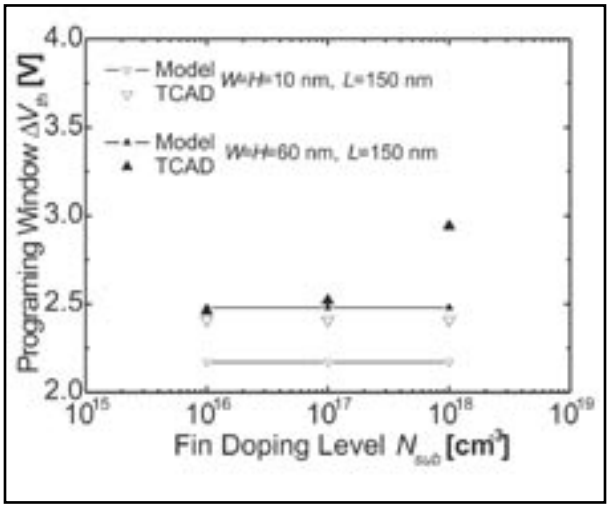

Fig. 7. Comparison between the programming windows obtained by the TCAD and by our model with different fin doping level. Both a large and a small fin device are represented, however the doping level of the fin does not impact much on the device performance at least up to the case of W = L = 60 nm and Nsub = 1018 cm-3, where we deal with a partiallydepleted device.

The problem of perfect Dirichlet boundary condition at source drain is alleviated by the consideration of epitaxially raised source/drain junctions. As shown in Fig. 2a, the ideal device used for the comparison with TCAD simulation does not have raised source and drain junctions. However in actual devices the source and drain are normally raised in order to diminish access resistance, thus their geometry approaches the assumption of perfect Dirichlet boundary conditions made in our analytical model.

V. Conclusion

We have presented an original semi-analytical model that efficiently describes important electrical features of complex 3D SOI FinFLASH memory structures operating in weak inversion. The proposed model does not need any fitting parameter and shows a good agreement even for doped fully depleted devices. Indeed, this model could be an effective tool to further investigate the electrical performance (i.e. multibit, multilevel, etc.) of different architectures of FinFLASH cell (i.e. SONOS, nanocrystal-based, etc.), without the need of implementing time consuming numerical simulation.

Acknowledgment

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TCAD Modeling and Data of NOR Nanocrystal Memories

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Introduction

It is widely believed that the scaling of standard Flash devices will face in a near future several limitations, due to the high voltage requirement of the program/erase and the stringent charge storage requirement of the dielectrics [1]. Among the possible solutions to push further the scaling limits of standard technologies, Si nanocrystal (Si-NC) memories are one of the most promising. It has been shown that thanks to the discrete nature of Si-NC, thinner tunnel oxide can be used (allowing lower operating voltages), without compromising the reliability [2, 3]. Indeed, a first understanding of the Si-NC memory behaviour can be achieved through simplified/semianalytical models [4, 5, 6]. Nevertheless, these approaches are not enough accurate to allow the optimization of the technological parameters, especially for NOR cells, written by channel hot electron (CHE) injection. To this aim, more complex numerical models, which take into account twodimensional (2D) or even three-dimensional (3D) effects, should be used.

In this work, we present TCAD simulations of NOR NC memories performed with commercial tools, which allow for a good understanding of the impact of the localized charge on both electrostatics and dynamics of the cell. Correlations with experimental results will be also presented.

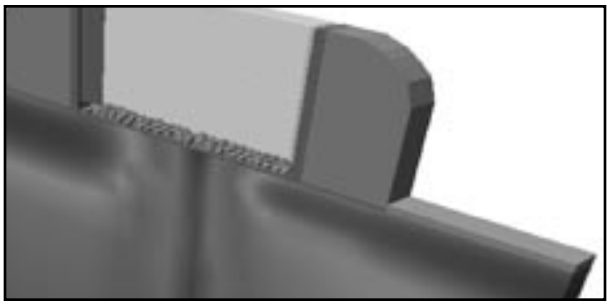

Figure 1. View of the 3D simulated structure with randomly distributed nanocrystals.

I. Devices and Simulation Tools

Devices tested in this work are NMOS memory cells with a layer of LPCVD (Low Pressure Chemical Vapor Deposition) Silicon nanocrystals acting as floating gates. The mean diameter of nanocrystals is about 5 nm and the density is 1E12 dots/cm^2. The tunnel and top oxide dielectrics are thermal S_iO_2 and HTO (High Temperature Oxide) with a thickness of 4 nm and 10 nm, respectively. The gate length of the cell is 0.23 μm and the width is 0.16 μm (corresponding to the ATMEL 0.13μm NOR Flash technology node).

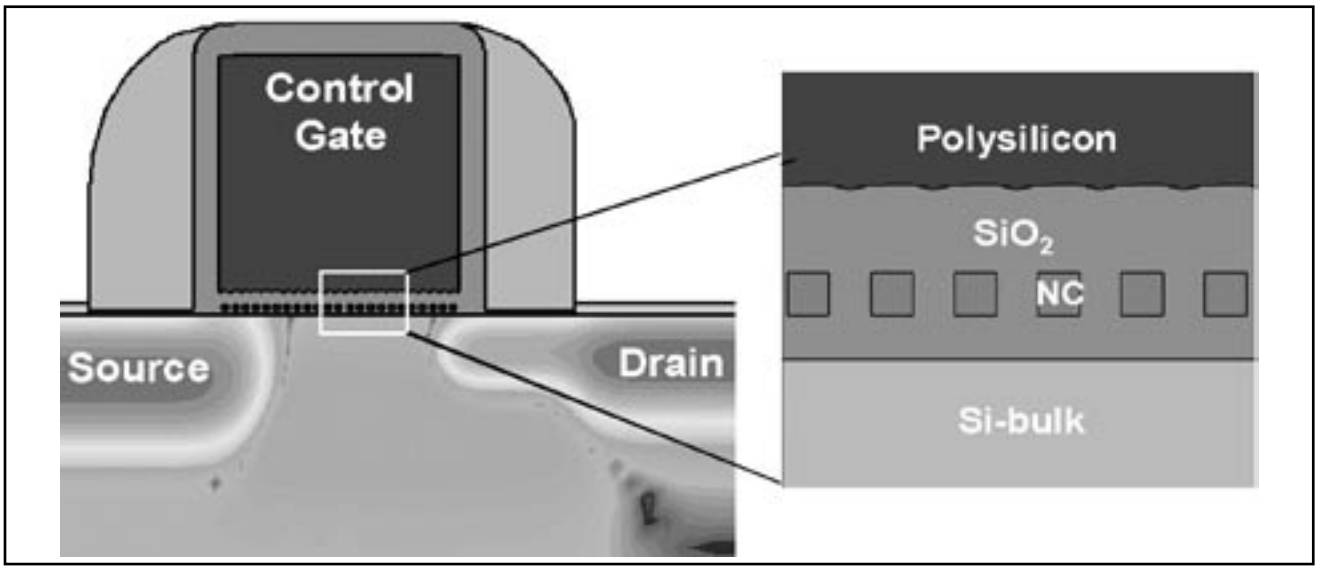

Figure 2. View of the 2D simulated structure with ordered nanocrystals.

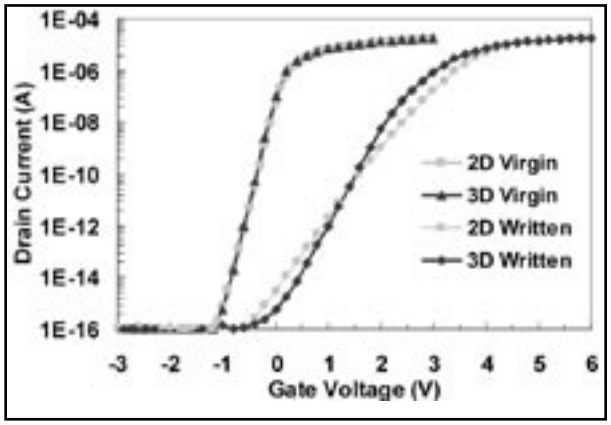

Figure 3. Simulated transfer characteristics of the 3D and 2D structures, in the virgin and written states. Reading Vds = 0.1V.

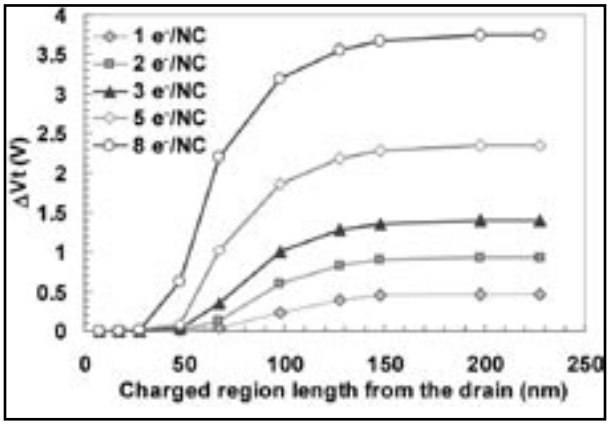

Figure 4. Simulated programming window as a function of the charged area length (extending from the drain junction). Reading Vds = 1V.

Two- and three-dimensional simulations have been performed with commercial TCAD tools [7]. Structures fed to the device simulator, including doping profiles, were obtained from 2D process simulations (2D profiles were then extruded in the third dimension for 3D simulations). In the simulated devices, nanocrystals are approximated as metallic cubes with 5 nm edge and a density of 1E12 dots/cm^2.

II. Electrostatic Simulations

A. Comparison between a 3D "random-distributed" NC memory cell and a 2D "ordered" NC memory cell

A three-dimensional structure, where the embedded nanocrystals are randomly distributed (both along the device length and width), was firstly simulated (see Fig.1). Indeed, this structure resembles the actual device, but 3D simulations imply high computational burdens. To bypass this limit, a 2D NC device (see Fig.2), where the embedded nanocrystals are ordered (i.e. equally spaced along the cell length and extending like rod structures along the device width) was also simulated. Due to the ordered nanocrystal configuration, in 2D uniformly charged devices, the trapped electrons give rise to a wave-like modulation of the surface potential along the device length, while creating a uniform potential barrier over the device width. An agreement between electrical results of the 2D and 3D structures should be quantitatively demonstrated.

Fig.3 shows a comparison between the transfer characteristics (in the virgin and written states) of these two structures. In the written state, the nanocrystals located in a region extending about 80nm from the drain junction on the active channel have been uniformly charged (with 10 electrons per dot). This situation corresponds to memory cells operating in NOR configuration, written by channel hot electrons. Note that, in order to have the same surface charge density in 2D and 3D simulations, the number of electrons trapped in 2D nanocrystals (which, as already said, extend like rod structures all along the device width) is normalized, by means of a multiplicative factor which takes into account the real nanocrystal coverage ratio along the device width [4]. From Fig. 3, it clearly appears that the 2D and 3D structures have similar behaviours. Based on these results and due to the significant improvement in computational time for 2D structures with respect to the 3D ones, the former has been the preferred choice for the next simulations.

B. Influence of the charged region length on the memory programming window

Electrical simulations of memory devices with different uniformly charged region lengths, extending from the drain junction (i.e. different numbers of uniformly charged NCs), and different numbers of electrons per dot, were performed (see Fig.4). It clearly appears that the memory programming window (ΔVt) saturates well before the charged region covers the entire memory channel. For a 0.23 μm cell length, a charged region extending from the drain junction toward the channel of about 150 nm makes the ΔVt saturate to a value which linearly depends on the number of trapped electrons per dot (linked to the writing bias conditions and to the dot size [8]). Indeed, this result suggests that, to achieve high memory ΔVt, the HE writing conditions should take care of optimizing the current injection peak in a region close to the drain junction, more than trying to extend the electron injection all over the channel.

III. Hot-Electron Programming Simulations and Experimental Data

The 2D device simulations were performed with ***ATLAS*** TCAD commercial tool [7]. Fig. 5 illustrates the comparison of simulated programming injection currents of a NC cell under hot electron writing for different transport models: energy balance transport model [9, 10] and drift-diffusion model [11]. In both cases, for the hot

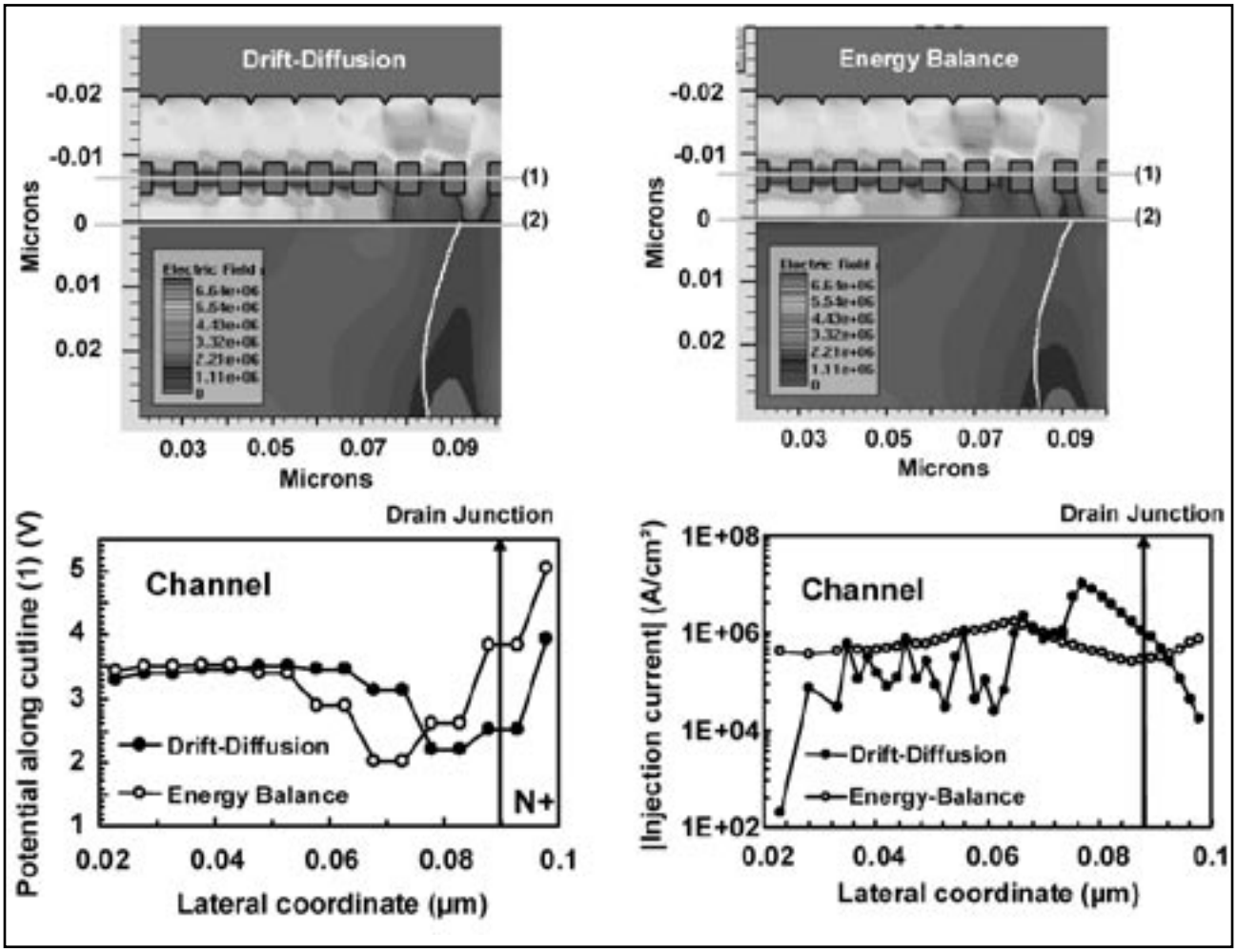

Figure 5. Comparison of 2D simulated nanocrystal devices under hot electron programming (Vdstress=4V, Vgstress=8V, tstress=10μs, Vbulk=0V, Vs=0V) with different transport models in the channel (drift diffusion and energy balance). Up: Electric fields in the simulated device. Down: Left - Potential cuts in the charged dots (1); Right – Injection current density distributions (at 1nm from the Si/SiO2 interface (2)).

electron injection in the dots, the lucky electron model [12] was used. When the lucky electron model is associated with the energy balance model, an effective electric field depending on the carrier temperature is calculated. In agreement with the literature [13], we observe that the drift-diffusion model fails to predict the injection current in the channel region. In particular, the simulated program efficiencies based on the drift-diffusion model resulted much lower than the experimental ones (especially at low-medium voltages), essentially due to the fact that the injected charges are confined in NCs located very close/above the drain junction, and so not affecting the device threshold voltage. Note that, this behaviour is much less critical in the case of standard Flash memories, where the injected charges are immediately distributed in the continuous floating gate whatever the injection point position.

A good agreement between simulations and experimental data was obtained by using the energy balance transport model [9, 10] plus the lucky electron model [12] for the electron injection in the dots. Figs. 6 and 7 show the simulated transfer characteristics of written NC memory cells, parameterized as a function of the stressing time (tstress) and of the stressing gate voltage (Vgstress), respectively. In the Insets of the same figures, the simulated programming windows are compared with corresponding experimental results obtained on NC cells. As we can observe in Fig.8, the lateral location of the largest charged NC remains the same for different Vg stresses. On the other hand, similar analyses with respect to the stressing time (see Fig.9) show that the charges which are progressively trapped in the NCs modify the local barrier and shift the current injection point toward the channel. Fig.9 also reports a potential cut among NCs, showing that the stressing time which corresponds to charged NC located far from the drain junction also corresponds to the higher programming window (see Fig.7).

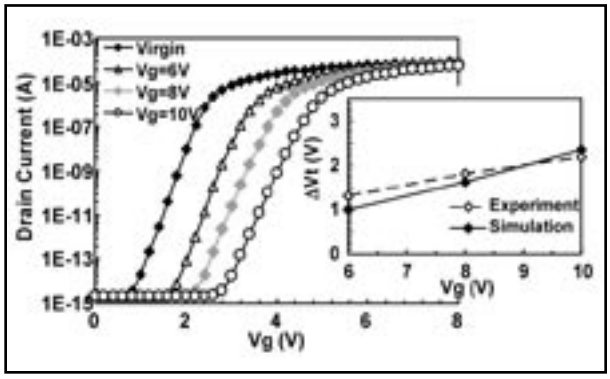

Figure 6: Simulated Id-Vg of the 2D device, virgin and written by HEI with different writing gate voltages (tstress=10µs, Vdstress=5V, Vbulk=0V, Vs=0V). Device is read at Vds=0.5V. Inset: Comparison of simulated programming windows (ΔVt @ Id=10-7A) and corresponding experimental ones.

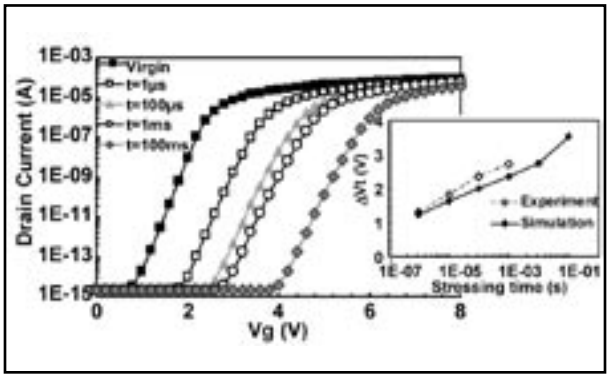

Figure 7: Simulated Id-Vg of the 2D device, virgin and written by HEI with different writing times (Vdstress=5V, Vgstress=8V, Vbulk=0V, Vs=0V). Device is read at Vds= 0.5V. Inset: Comparison of simulated programming windows (ΔVt @ Id=10-7A) and corresponding experimental ones.

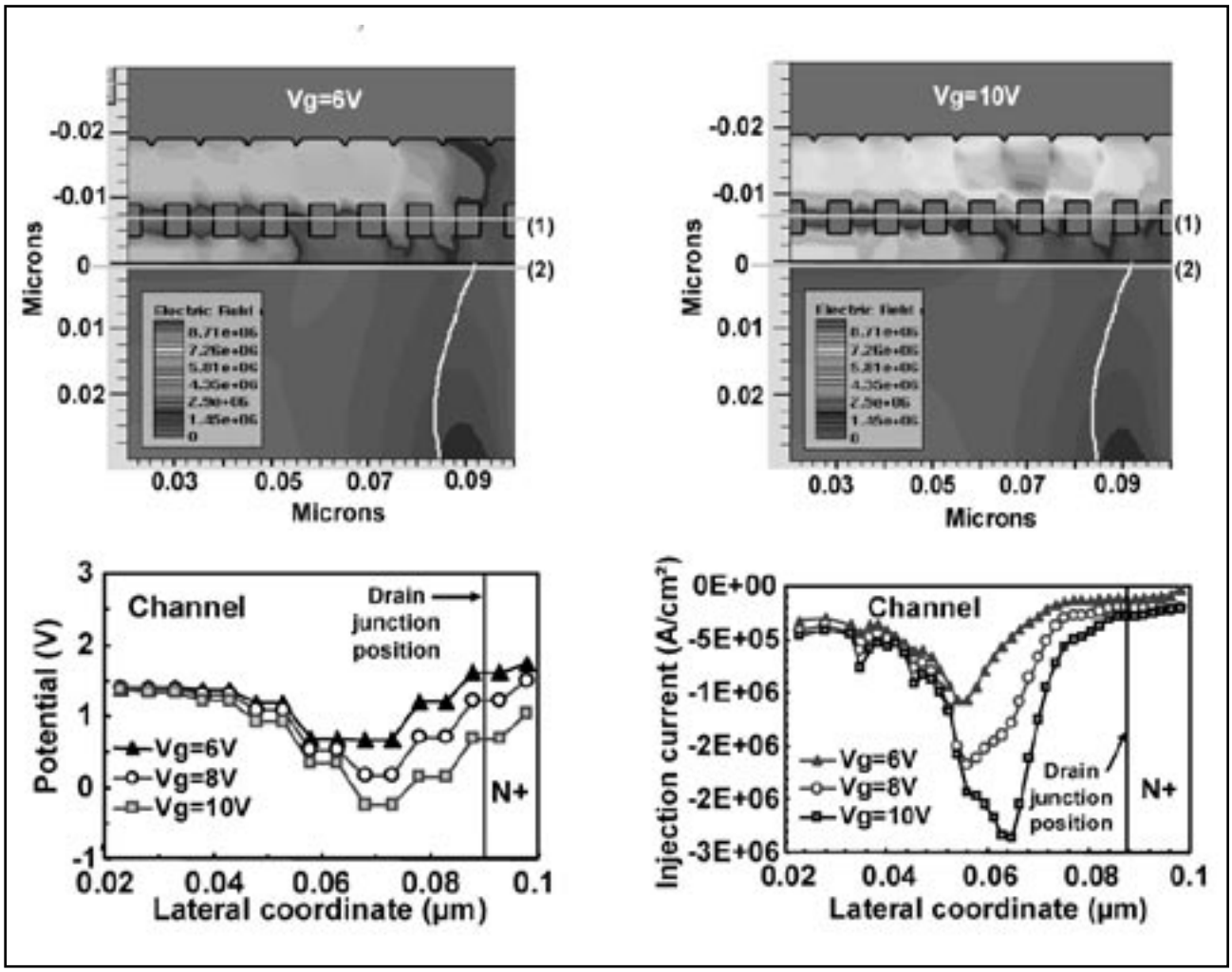

Figure 8. Up : Electric fields in 2D devices corresponding to Fig.6 (i.e. different writing gate voltages, Vdstress=5V, tstress=10µs, Vbulk=0V, Vs=0V). Down: Left - Potential cuts in the dots (1); Right – Injection current density distributions (at 1nm from the Si/SiO2 interface(2)).

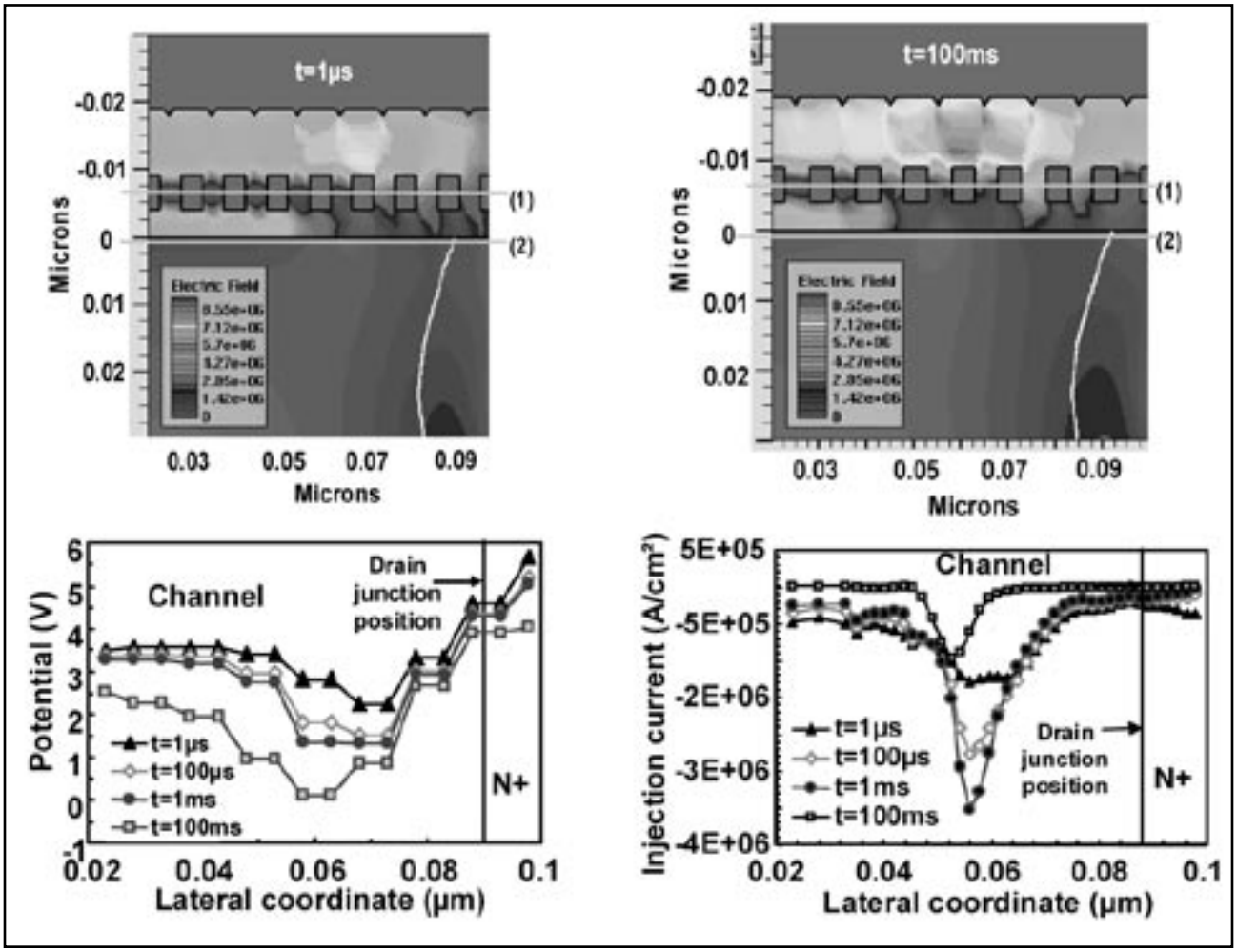

Figure 9. Up : Electric fields in 2D devices corresponding to Fig.7 (i.e. different writing times, Vdstress=5V, Vgstress=8V, Vbulk=0V, Vs=0V). Down: Left – Potential cuts in the dots (1); Right – Injection current density distributions (at 1nm from the Si/SiO2 interface (2)).

IV. Conclusion

Two- and three-dimensional TCAD simulations of NOR nanocrystal memories have been presented. The electrostatic and dynamic behaviours of the cell have been studied and compared to experimental data. The key role of the position of the trapped charges along the channel length on the threshold voltage shift has been put in evidence. Indeed, this result is critical for NOR discrete-trap memories, where the HE injection is essentially aligned with the drain junction.

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Hints, Tips and Solutions

How Can I significantly Reduce Circuit Parasitics Netlist Extraction Time ?

SILVACO has recently released a new suite of parasitic extraction tools to meet the demands of state-of-the-art designers at cell, circuit and chip level. After having proved [1] [2] [3] the accuracy of these tools, SILVACO now focuses his attention to decrease the simulation time, by taking benefit from Multi-CPUs computing architectures.

The results presented here have been obtained with ***STELLAR***, a 3D-based Field Solver with full-chip capacitance extractor. The software uses an advanced numerical method, the so-called fictitious domain method, which is based on the decomposition of the simulation domain into sub-domains. The parallel version of ***STELLAR*** accepts a command line option -P n, which allows running the m sub-domains simulations in parallel on n CPUs (n being the number of requested CPUs). Simulations were done by STMicroelectronics Crolles France on a SunOS 5.8, 16 CPUs, Sun-Fire-V890. The layout used for this study had the following characteristics: 106x230 um^2 area, 7 metal layers and 6 via layers. In the following text and figures, the CPU time is the total on-CPU time as measured by a UNIX ps or top command, while the Wallclock time is the real-world time, as measured by a watch.

The decomposition algorithm is sufficiently robust to give a very limited (3%) variation of the capacitance with the number of sub-domains represented by a decomposition step d (Figure 1). High value of d correspond to a low number of sub-domains. It is also clear from Figure 1 that CPU time increases with d. As a consequence it was decided to set d to 1.91 corresponding to 90 sub-domains. It has been verified that for a given decomposition, the capacitance does not vary with the number of requested CPUs.

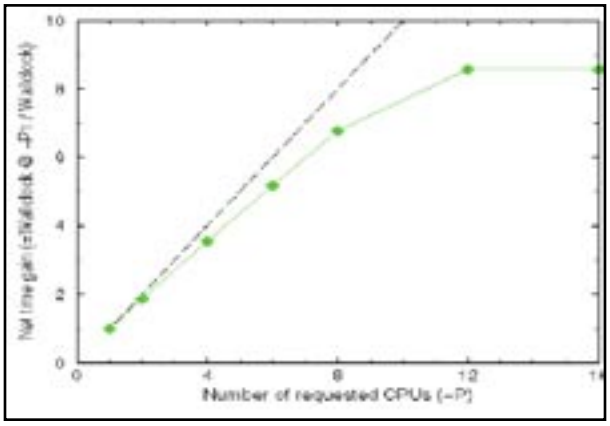

Figure 2. Time Gain versus number of CPUs. The dashed lines show an ideal parallelization

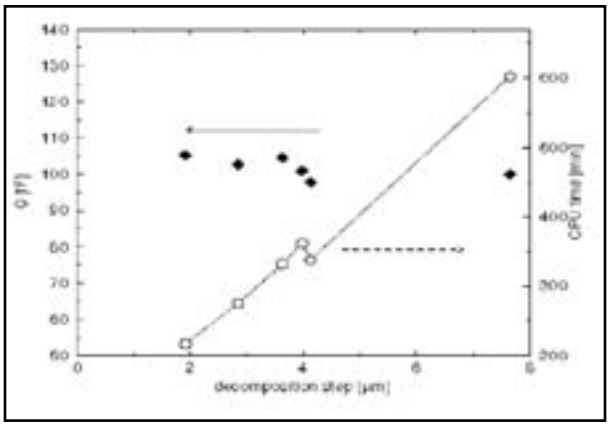

Figure 1. Capacitances and CPU time as a function of decomposition step d. 1 CPU used

As can be seen in Figure 2, the parallelization is very good (near the theoretical limit) for a number of requested CPUs around 8. Running on 12 CPUs leads to a gain time of a factor 9. The layout used for this benchmark was relatively small. The advantage of parallelization over a larger number of CPUs maybe even more advantageous for larger structures. This result is achieved easily (no preliminary optimization runs) if the decomposition step d is chosen such that a large number of subdomains is obtained (90 in this case). In other words the parallelization is fully exploited only if n is significantly lower than m.

Acknowledgements:

SILVACO wishes to thank STMicroelectronics Crolles France for its collaboration to this work.

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