

# Simulation Standard

Connecting TCAD To Tapeout

A Journal for Process and Device Engineers

## Inductance Optimization using 3D Field Solver based on Design Of Experiment Approach

### Abstract

A new 3D electromagnetic simulator coupled with a statistical analysis, for inductance loop optimization is presented. It allows RF designers to easily create inductor design by only specifying as inputs the desired inductance and Q factor for example and get as outputs layout parameters like radius, wire width, space between wires and numbers of coils. To do so, inductance simulations using Design of Experiments (DoE) approach are done and subsequent Response Surface Model (RSM) are generated. Performing an optimization on the RSM model a gds2 inductance loop layout is generated according to the user specified initial constraints and will be ready to use in a design of RF-circuits. Inherent to this new methodology the designers can now take into account process variations which is mandatory for current technology node.

### 1. Introduction

Up to a few Ghz, on-chip inductors are among the most critical components to design radio-frequency integrated circuits (RFIC). The main parameters that characterize an inductor are its self-inductance value  $L$ , its cut-off frequency and its quality factor  $Q$  (a good inductor has a high  $Q$ ). For on-chip inductors,  $Q$  is limited for example by the inductor's series resistance, the resistive loss (skin effect and proximity effect) and the current induced by the capacitive coupling to the ground plane and the substrate. In this context it is imperative to allow engineers to easily and accurately create any RF structure and give designers the flexibility to innovate new geometries simply by editing parameters such as radius, number of turns, width and spacing of coils. The aim of this paper is indeed to explain how this can be possible using a specific methodology based on Design Of Experiments approach in combination with a new field solver simulator.

### 2. 3D Electromagnetic Simulation

In this paper, we use the 3D electromagnetic field solver *QUEST*. *QUEST* is very accurate to design and characterize arbitrary 3D passive structures (inductance loop

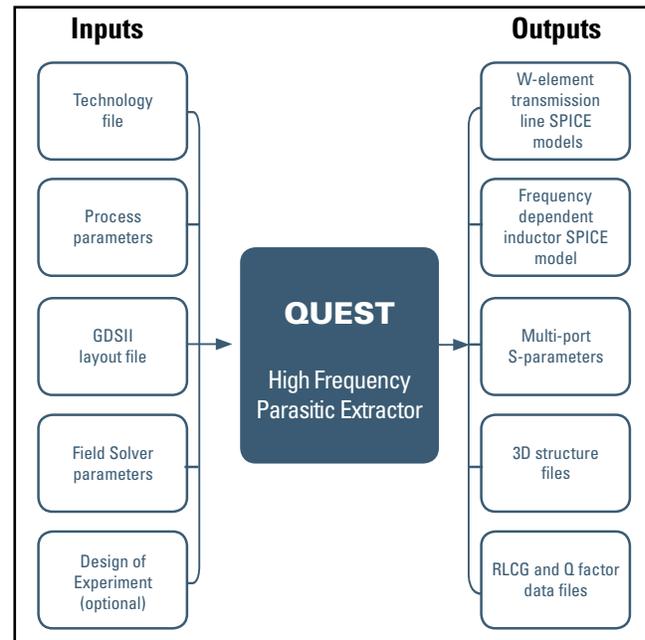


Figure 1. Inputs/Outputs of QUEST

for example) as a function of process and layout parameters. *QUEST* is mainly dedicated to simulate multi-level interconnections according to the current technology (typically up to 8 metal levels). Some conductors may be grounded (connected to a reference potential) or floating (not connected to any potential).

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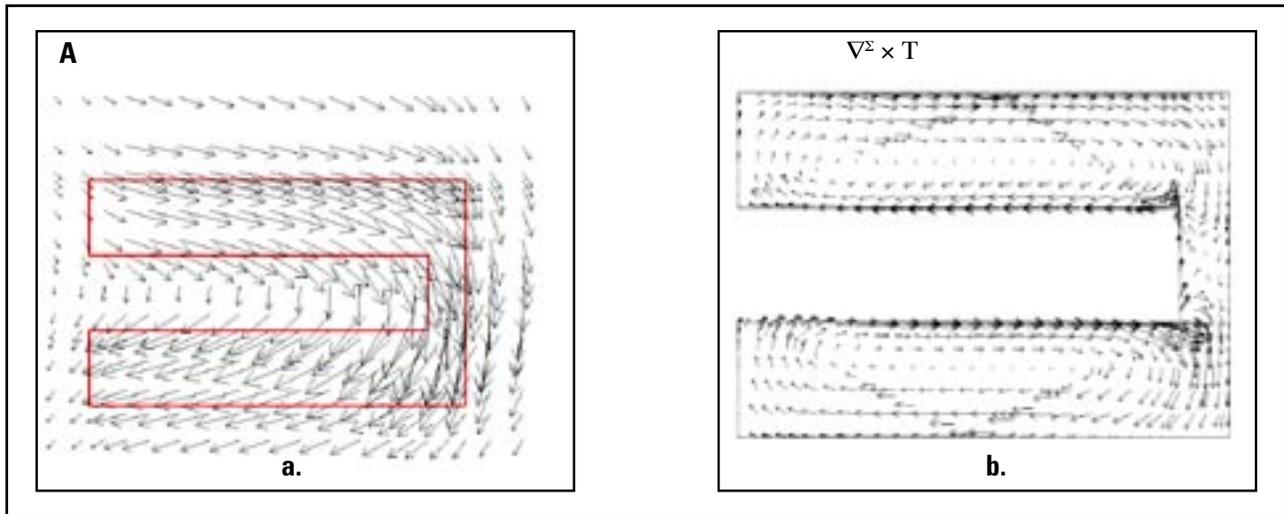


Figure 2. a. Magnetic Potential vector( $A$ ) and b. Density of Current ( $\nabla^2 \times T$ )

*QUEST* computes firstly the 3D structure resulting of the layout information, process and techno file inputs, then, after simulation, *QUEST* can give RLGC parameters, S-Y-Z-parameters, Q factor and spice model for inductance loop simulation and standard Spice W-element format for transmission line simulation (Figure 1). All these output parameters are function of the frequency. These results are stored in a database and can be used in post-treatment for statistical analysis for example.

### 3. Field Solver

*QUEST* is based on a 3D field solver elaborated in collaboration with CEA-LETI[1][2]. We use an original formulation of the Quasi-Static Maxwell equations where the problem is separated in two parts, an impedance and a capacitance part.

The impedance problem is written using a  $(A, T^2)$  formulation [3], where  $A$  is the magnetic vector and  $T^2$  is an equivalent electric potential vector defined on the conductors surface,  $\mu$  the mobility,  $w$  the frequency and  $\sigma$  the conductivity.

$$\nabla \times \mu^{-1} \nabla \times A - \nabla^2 \times T^2 = 0$$

$$\nabla^2 \times (\sigma^2)^{-1} \nabla^2 \times T^2 + jw \nabla \times A = 0$$

The magnetic potential vector  $A$  is calculated using edge finite elements [4] on a 3D regular grid (Figure 2a). The electric potential vector is calculated using scalar P1 elements on a triangle meshing of the conductors surfaces (Figure 2b).

The capacitance problem comes from the equation

$$\nabla^2 \times (z^2)^{-1} \nabla^2 \phi^2 = jw p^2$$

where  $\phi^2$  are the surface potential and the surface electric charge respectively.  $z^2$  is a local impedance given by the impedance problem. It is solved using a fast and accurate computation method so called « fictitious domain method » [1].

### 4. Inductance Loop Validation

*QUEST* results have been validated in collaboration with ST Crolles on realistic inductors using advanced CMOS processes (0,12um technology, 6 metal levels). *QUEST* directly uses real gds2 files and can compute any type of geometries (square, spiral, octagonal inductors). Figure 3 presents a 4-turns inductor structure computed by *QUEST*. The real process with a quasi unlimited numbers of dielectric layers can be directly taken into account without any simplification.

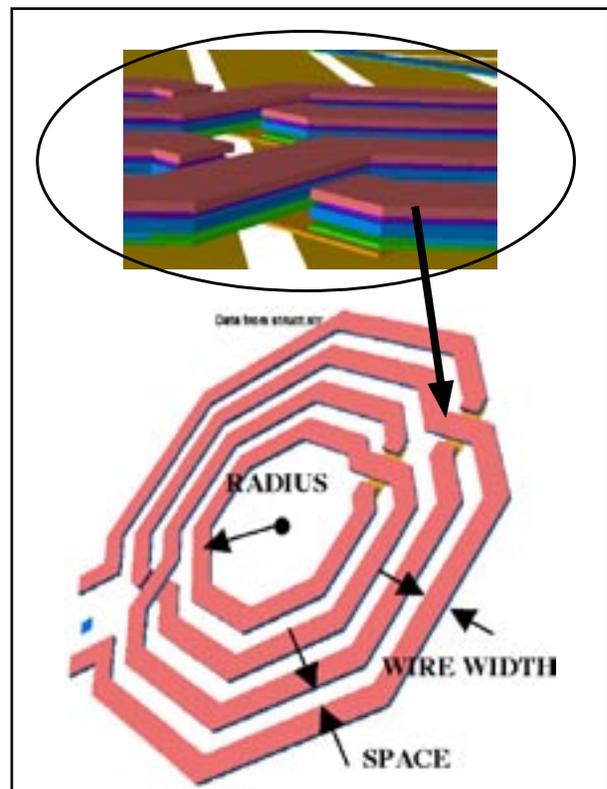


Figure 3. 4 turns inductance loop on a patterned ground plane (not shown here).

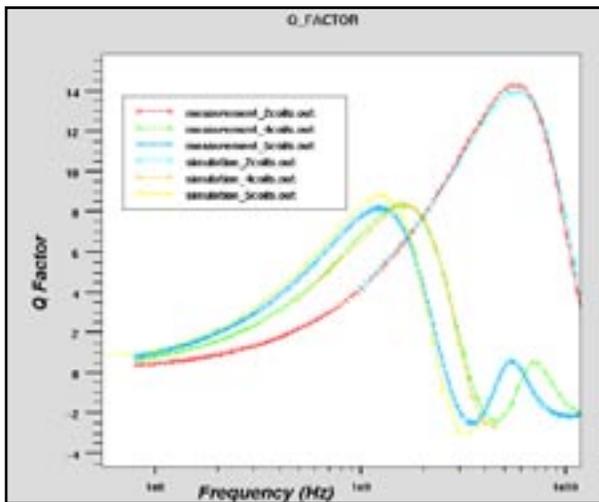


Figure 4. 2, 4 and 5-turns inductor Q factor versus frequency

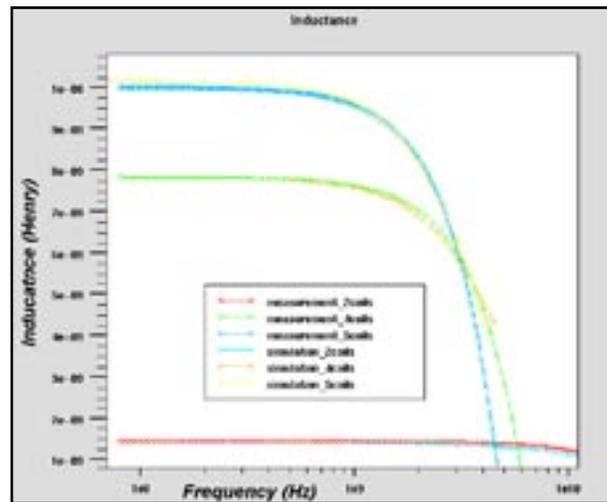


Figure 5. 2, 4 and 5-turns Inductance versus frequency

We made comparison between measurements and simulations on a 2-turns, 4-turns and 5 turns inductors. As can be seen in Figure 4 and 5, simulations and experimental data match very well. The Q-factor was given by  $Q = -\text{Im}(Y_{11}) / \text{Re}(Y_{11})$  and L extracted from the imaginary part of  $1/Y_{21} = -(R + j\omega L)$ . Different types of inductors have also been validated but not shown here. The simulations of the inductance loops were performed on a Linux PC AMD 2800 64 bits. The simulation time for the 2 turns inductance shown in Figure 5 was 10min with 21 frequency points.

## 5. Inductance Synthesis and Optimization

After having validated the field solver, we will use and show an original methodology to design inductance loop based on simulation results instead of experimental data from real wafers (which is long to have and very expensive). As an example, we want to design a gds2

inductance loop layout, based on a 0,12um technology from ST, having as constraint a minimum area and a specific value of inductance L. For that purpose, Design of Experiment (DoE) approach and parameterized gds2 layout have been used. Indeed the idea is to make a variation of layout parameters such as radius, number of coils, width and spacing and run the simulations using a DoE for subsequent modeling using Response Surface Model (RSM)[5]. Performing an optimization on the RSM model gds2 inductance loop layout can be generated according to the user specified initial constraints and will be ready to use in a design of RF-circuits. To achieve this goal, the first step is to create a parameterized gds2 layout. For that purpose, the script language of a layout editor (Expert from Silvaco) was used to create a generic parameterized inductance gds2 layout as a function of layout parameters (Radius, Wire Space and Width, Number of coils) as shown in Figure 4. Now we want to vary layout parameters of the inductance previously defined. The frequency range for the simulation was set between 100Mhz to 9Ghz. The wire width was varied from 4um to 12 um, the space between wires from 4um to 10um, the number of coils from 2 to 4 and the radius between 50um to 150um. A third order full factorial DoE has been used for the layouts parameters. 27 different layouts were created. Different RSM models were generated (L, C, Q, S-Parameters ...) as a function of layout parameters (space, width, number of coils, radius). By using the RSM model for the inductance, very interesting information for the designer can be found. For example isosurface values (Figure 6) of inductance as a function of radius, number of coils and wire width, allow to have a first idea of the area needed to design the inductance layout. Another interesting information for the designer is the correlation between parameters. Indeed the inductance value is highly correlated to the radius and number of coils and less to the wire width and wire space as shown in Figure 7.

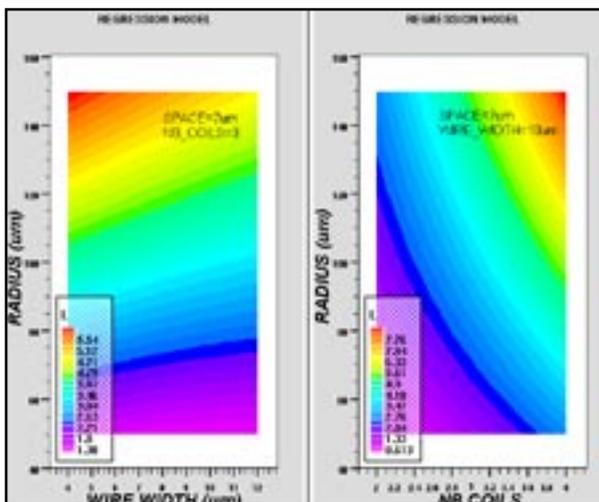


Figure 6. Inductance variation as a function of wire width, radius and number of coils.

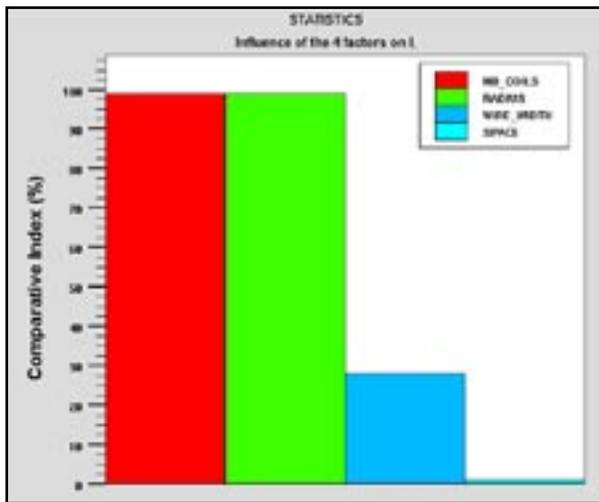


Figure 7. Pareto graph showing the correlation between the inductance value and the layout variables.

This is a good indication for the designer in order to focus his effort in optimizing the preponderant parameters. The ultimate goal is to perform automatic synthesis of the “ideal” gds2 inductance layout that the user has to design for a specific circuit. The aim is to find, for example, the set of layout parameters to obtain an inductance value of 2nH using a minimum surface of silicon for a circuit working at 2Ghz. For that an optimization is performed based on the inductance RSM model and the following results are obtained: NBcoils=3, Width=4.8um, Space=5.2um and Radius=60um. The designer now has at his disposal a complete inductance layout corresponding to his need. He can easily perform a second optimization without running any additional simulations in specifying for example in this case a specific value for L and Q factor or even use a desirability function like the maximum of L and a fixed value for the Q factor.

He will then obtain in a few seconds a new gds2 inductance layout corresponding to what he wants.

After having defined his nominal layout parameters the designer may want to study the impact of the frequency and the variation of process parameters. For example the Q-Factor is shown, in Figure 8, as a function of the frequency for the layout with its nominal values previously obtained (NBcoils=3, Width=4.8um, Space=5.2um and Radius=60um)

The designer can easily see the variation of the characteristics of the inductance anticipating the needs of his circuit to work at a different frequency.

Using the same concept as previously defined we can also make variation of process parameters (Thicknesses of dielectrics or metals, permittivity ..) in order to predict the output parameters of the inductance (L, Q, S-Parameters ..) as a function of process variation. This

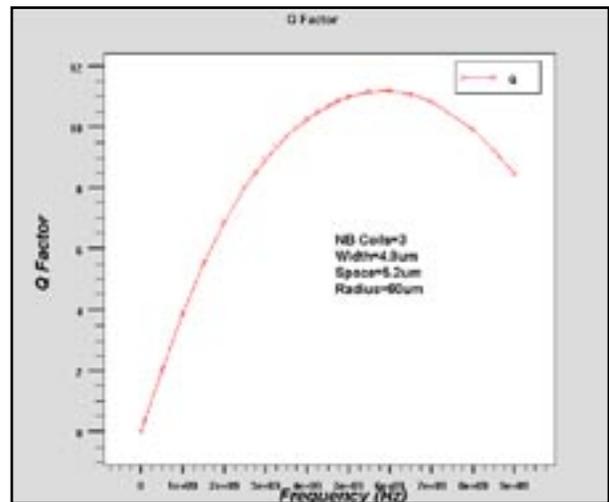


Figure 8: Q factor as a function of the frequency.

is very interesting for designers in order to integrate the fab process variation in the design. After having modeled the desired outputs (Q-factor for example) as a function of process parameters we can use Gaussian distribution given by the foundry for each process parameters. This distribution correspond to the deviation of each process parameters as compared to their nominal value due to the variation of process condition in the fab (calibration of machines, temperature variation ...) Then, we include for each process parameters the corresponding distribution in the RSM model. As a result we are able to determine what is the deviation of the output parameters (Q-factor for ex) including the process variation from the foundry. 4 process variables have been used in this example : Metal5 and Metal6 thicknesses and inter metal dielectric IMD4 and IMD5 thicknesses as illustrated in Figure 9. The domain of variation of these process parameters are shown in Table 1. A third order full factorial DoE has been used leading to 81 simulations.

Sensitivity analysis shown that the Q-factor is highly dependant on Metal5 and Metal 6 thicknesses (Figure 10d). A Gaussian distribution for each process parameters have been set as input in the RSM model for Q-factor, R and L, with a standard deviation of +/- 10% as compared to their nominal value.

	Min	Nominal	Max
M5 Thickness (um)	0.25	0.35	0.45
M6 Thickness (um)	0.86	0.96	1.06
IMD4 Thickness (um)	0.26	0.36	0.46
IMD5 Thickness (um)	0.26	0.36	0.46

Table 1: Domain of variation of process parameters.

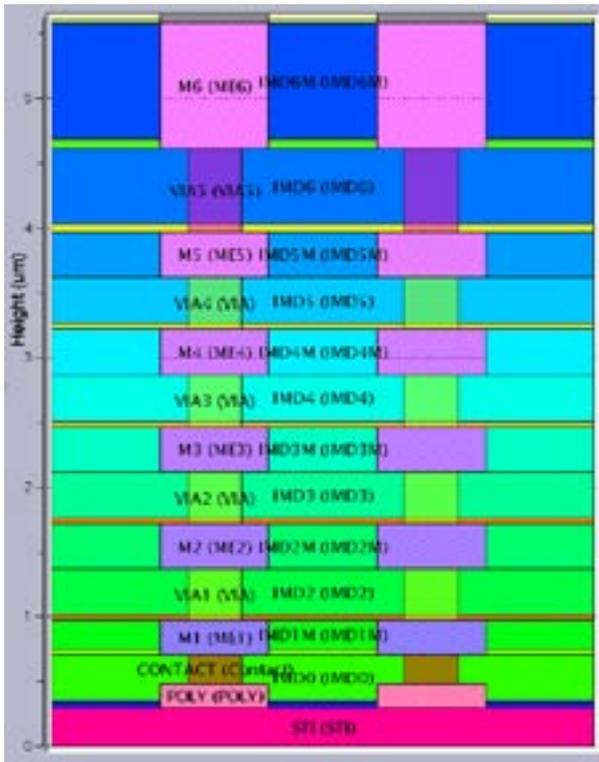


Figure 9: 0.12um ST Process description.

One can observe in Figure 10a a Gaussian distribution of the Q-factor with a mean value of 6.86 and a standard deviation of 0.225. This variation is mainly due to a change of the resistance as a function of process parameters (Figure 10b) whereas the inductance does not vary (Figure 10c). Based on these results, the designer has a better understanding of the behavior of his inductance versus the process variation and thus can take them into account during the design. In this example, a +/- 10% of Metal5 and Metal6 thickness variation will result in +/- 3.2% on the Q-factor as shown in Figure 10 a

## Conclusion

This article presented a new field solver simulator based on a original numerical method. Complex and complete inductance layout can be simulated very accurately. Thanks to the speed of this new simulator and integrated DoE feature, statistical analysis (meaning 10 to 100 simulations) is now possible in a only few hours. We have established a completely new approach to design inductors. Designers can now perform inductance synthesis and also include process variation in their design for the first time in realistic simulation time.

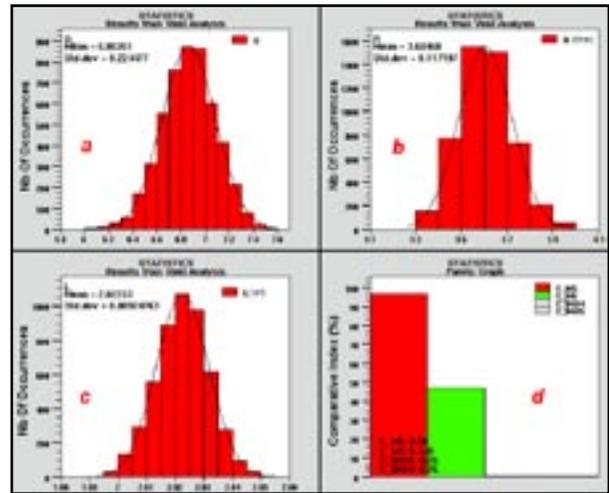


Figure 10: a. Q-factor, b. R and c. L distribution resulting from a +/- 10% variation on process parameters. d. sensitivity analysis. The frequency was set to 2Ghz.

## Acknowledgments

We acknowledge STM Crolles to have provided measurements and support to accomplish this work.

## References:

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# ATHENA/Optolith Simulation of Proximity Lithography

## 1. Introduction

Photolithography simulation is a very important part of TCAD. Accurate and predictive lithography simulation saves time and money spent on development and calibration of semiconductor technology processes. Photolithography simulation has also become a critical element of modern design for manufacturability (DFM) flows. Most lithography simulators are focused on resolution enhancement for projection imaging. This “standard” lithography technology is getting more expensive for each subsequent technology node. The proximity printing (i.e. imaging without reduction lens) is obviously more cost effective in printing relatively big features on micron scale. This method is effectively used in many applications, e.g. power device and flat panel display manufacturing. This paper briefly discusses implementation and use of proximity printing module in *ATHENA/Optolith*.

## 2. Proximity Lithography

Proximity lithography is used to print images without expensive projection systems. The scheme of proximity lithography system is shown in Figure 3.

Light illumination of the mask creates the diffraction pattern in the resist film placed on some distanced (called gap) from the mask plane. Due to the diffraction effects in the gap, the aerial image in the resist film is a distorted representation of the mask shapes. The extend of distortion depends on the gap size as well as on the radiation wavelength and size and shape of the mask features.

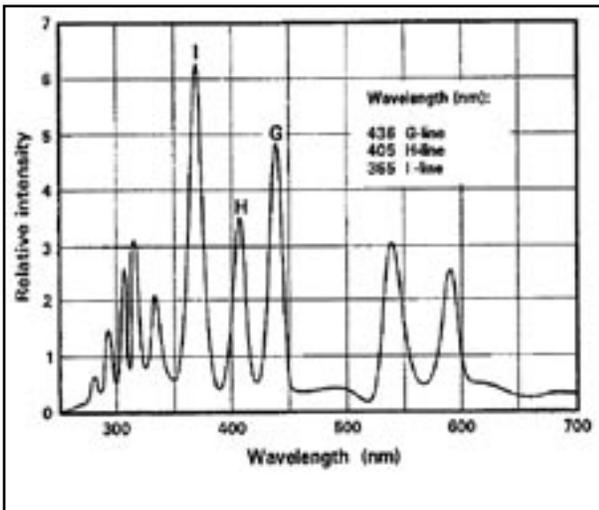


Figure 2. Spectrum of a high pressure Hg lamp.

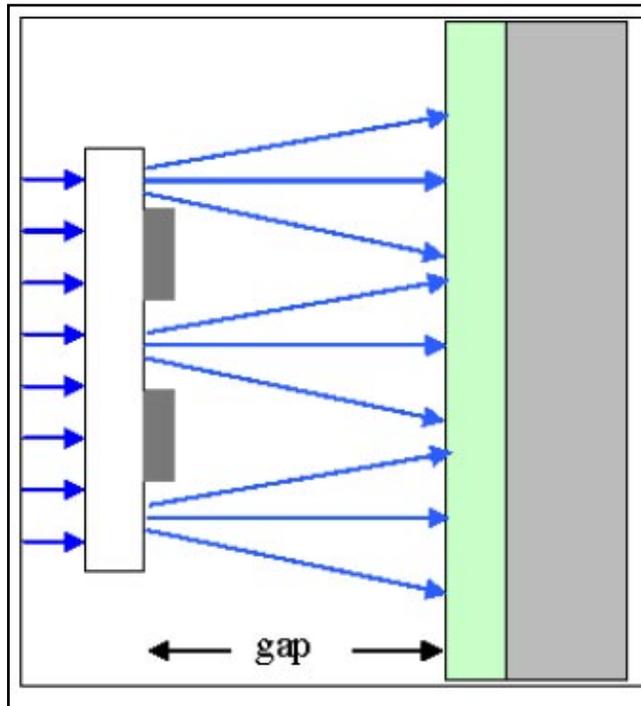


Figure 1. Scheme of proximity optical system

The broadband illumination is typically used for proximity printing. Figure 2 shows the light spectrum of a high pressure Hg lamp. In proximity lithography simulation this spectrum could be approximated by multiple exposure method in which images from main lines (i-, h-, and g-lines) could be superimposed.

## 3. Simulation Model and Parameters

*Optolith* simulates all four key steps of the photolithography processing: imaging module calculates aerial image of the mask features; exposure module simulates light propagation through photoresist and calculates photo active component (PAC) distribution; post-exposure bake module simulates redistribution (diffusion) of PAC; and development module calculates removal of exposed photoresist. The last three modules are the same for projection and proximity lithography, while a separate imaging module is implemented for proximity printing. Proximity imaging is invoked by specifying parameter GAP (the distance between mask plane and resist surface) in the IMAGE statement.

The proximity lithography image is calculated by the Fresnel diffraction using Fast Fourier Transform (FFT). The simplified version of Beam Propagation Method

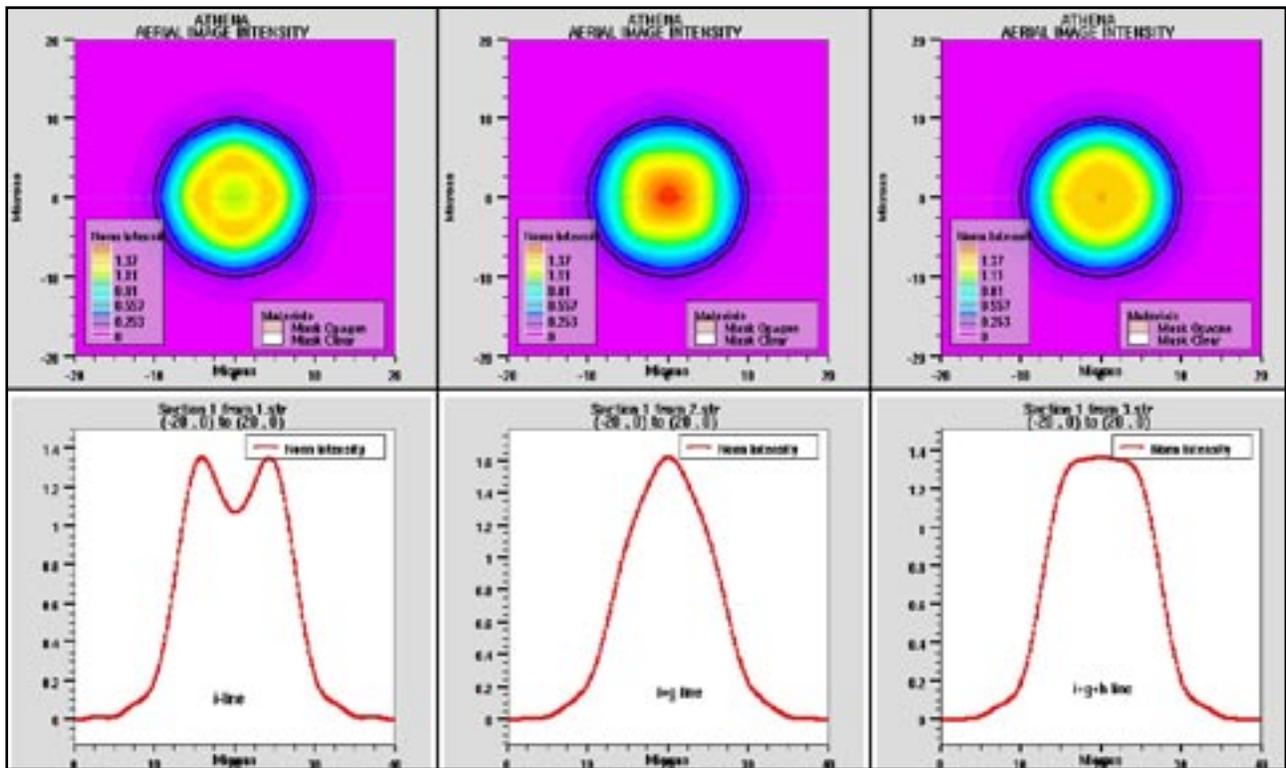


Figure 3. Simulated aerial image intensity.

(BPM) is used to describe light propagation through the gap. Unlike more complicated BPM in photoresist, in this case the gap is filled with homogeneous material, so refractive index does not depend on coordinates in the gap. The model is implemented for rectangular and circular masks as well as for masks consist of one or several rings. The parameters X.CIRCLE, Z.CIRCLE, RADIUS, RINGWIDTH, and MULTIRING in the LAYOUT statement can be used to specify the circular or ring mask features. Also, the half-tone masks can be specified by the TRANSMIT parameter in the LAYOUT statement.

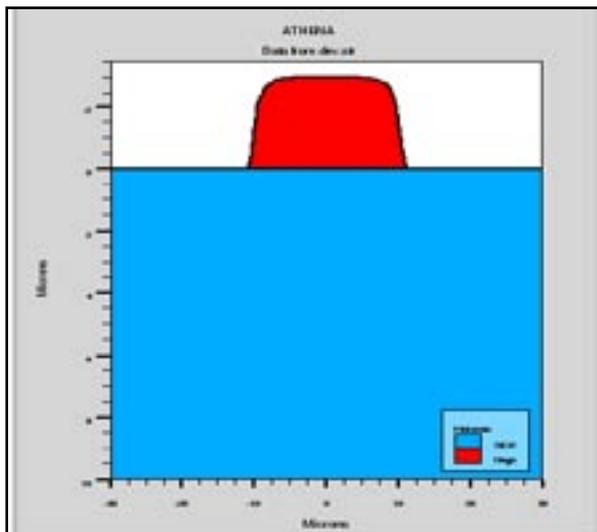


Figure 4. Simulated resist shape.

The example of aerial images of a circular mask with diameter of 20 microns is shown in Figure 3. Note, that as expected the best resolution is achieved for the broadband illumination approximated by combination of i-, h-, and g-lines.

The exposure A, B, and C parameters as well as Dill's development rate parameters  $E_1$ ,  $E_2$ , and  $E_3$  are usually provided by the photoresist manufacturers. However, they might be not provided for a specific broadband illumination. In this case some parameter fitting as needed. Several practical tools provided by Silvaco could be used for such fitting/calibration. These include *Optimizer* and DBInternal capabilities of *DeckBuild* and *Virtual Wafer Fab (VWF)* and its *Production Tools*.

Finally, Figure 4 shows an example of simulated photoresist shape obtained by proximity printing with approximated broadband illumination (shown in the third plot of Figure 3).

#### 4. Summary

This article describes capabilities of proximity printing module of *ATHENA/Optolith*. It is shown that the module can be successfully used for different aspects of lithography process design including optimization of exposure dose, light intensity, photoresist thickness, half-tone mask transmittance, mask shapes, and other parameters.

# Crosstalk Between Pixels of Organic Photo-Voltaic Devices

## Introduction

For various technological reasons, LEDs and as well as photo-voltaic devices frequently use PEDOT:PSS on top of ITO contacts as a hole injecting or hole collecting layer, respectively. However, due to the presence of this layer, a direct parasitic current path opens up between the ITO contacts of neighboring pixels.

Next to its influence on the optical properties of the layered device, the presence of the PEDOT:PSS layer between pixels may modify the potential profile in the active organic layer underneath and may therefore influence the lateral charge separation process in the illuminated device, causing optical induced electric crosstalk.

In this *Simulation Standard* we demonstrate the principal capabilities needed to simulate crosstalk between neighboring illuminated and dark pixels.

## Device and Models

The simulated structure of two neighboring pixels is shown in Figure 1. On top of an Aluminum layer, acting as common cathode, a blend of organic materials is deposited. This is followed by a 50 nm thick PEDOT layer of  $\rho = 5 \times 10^4 \Omega\text{cm}$  resistivity. The ITO electrodes for the two 100  $\mu\text{m}$  wide pixels have a thickness of 100  $\mu\text{m}$  and are

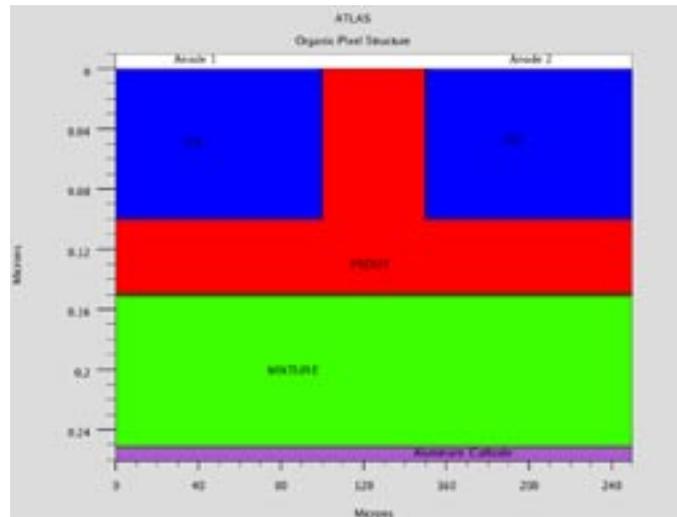


Figure 1. Device Structure – Neighboring Pixel. Note the very different scales along the horizontal and vertical directions.

separated by a 50  $\mu\text{m}$  wide gap filled with also PEDOT. The resistivity of ITO was taken to be  $\rho = 160 \Omega\text{cm}$ . The optical simulations were performed for monochromatic light at a wavelength of 550 nm. The optical properties for the layer materials used are taken from tabulated values stored in a user defined file. The corresponding data is shown in Figure 2.

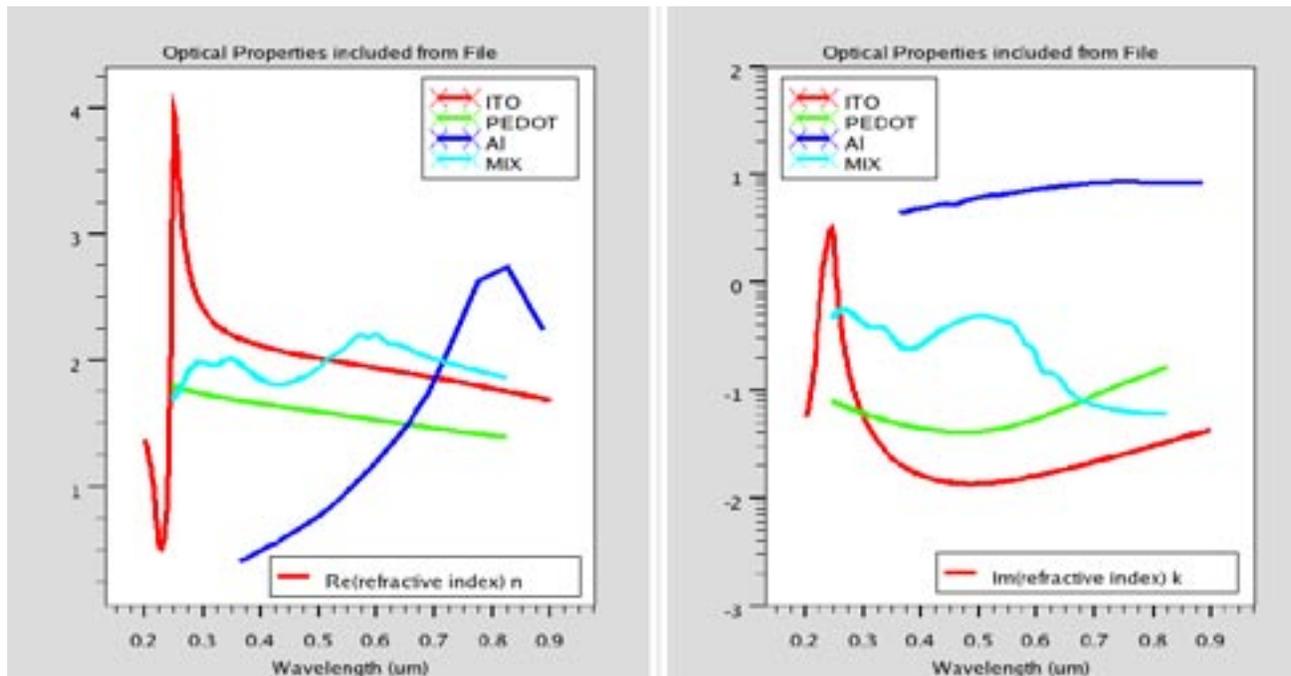


Figure 2. Optical Properties of layer materials used in the simulation.

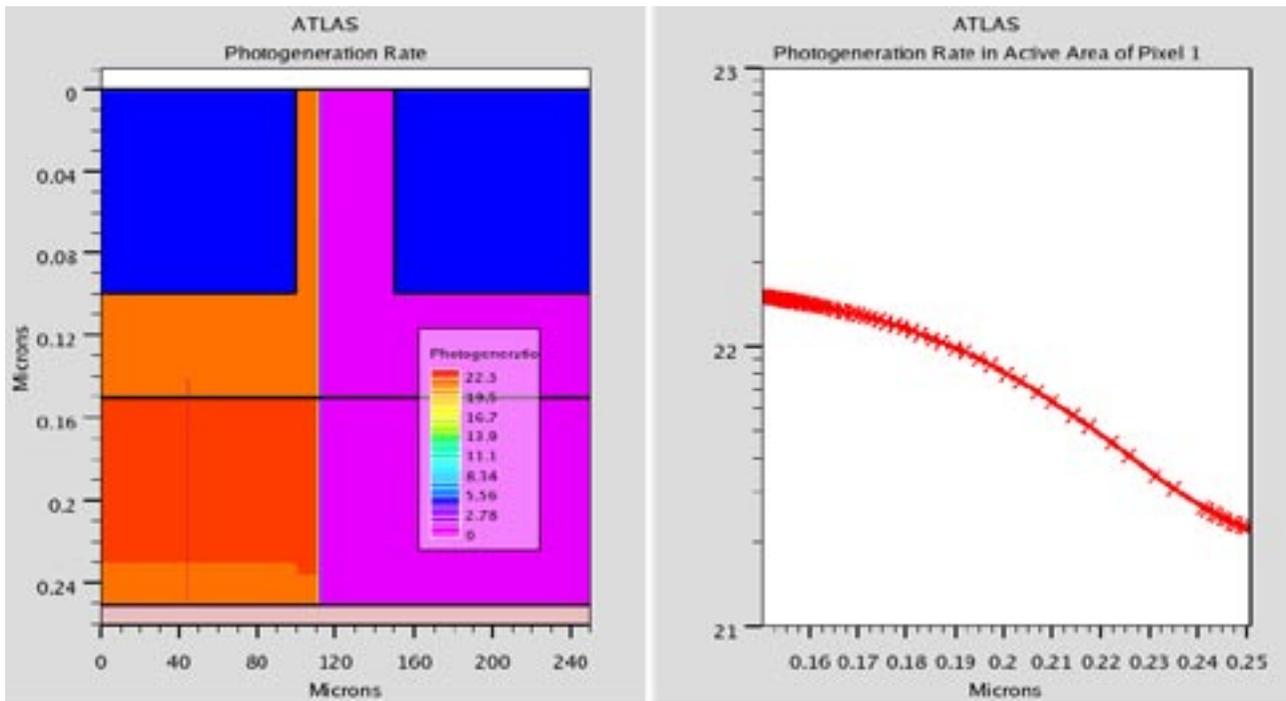


Figure 3. Illuminated Device: Photogeneration Rate along cutline in the illuminated Pixel.

Due to the fact, that layer thicknesses in such devices are typically in the same order of magnitude as the wavelength of the absorbed light, interference effects can be important. Such effects can be fully taken into account, using the implemented transfer matrix algorithm, utilizing the almost one-dimensional geometries of such devices. Although not exemplified here in detail, we note,

that this can be important to optimize the absorption profile in such devices. In the present example, the resulting absorption profile is shown in Figure 3. This results in IV characteristics for the neighboring pixels as shown in Figure 4. The characteristics of the left pixel is shown under dark and illumination conditions in the left part of the Figure. In the right graph, the current through the

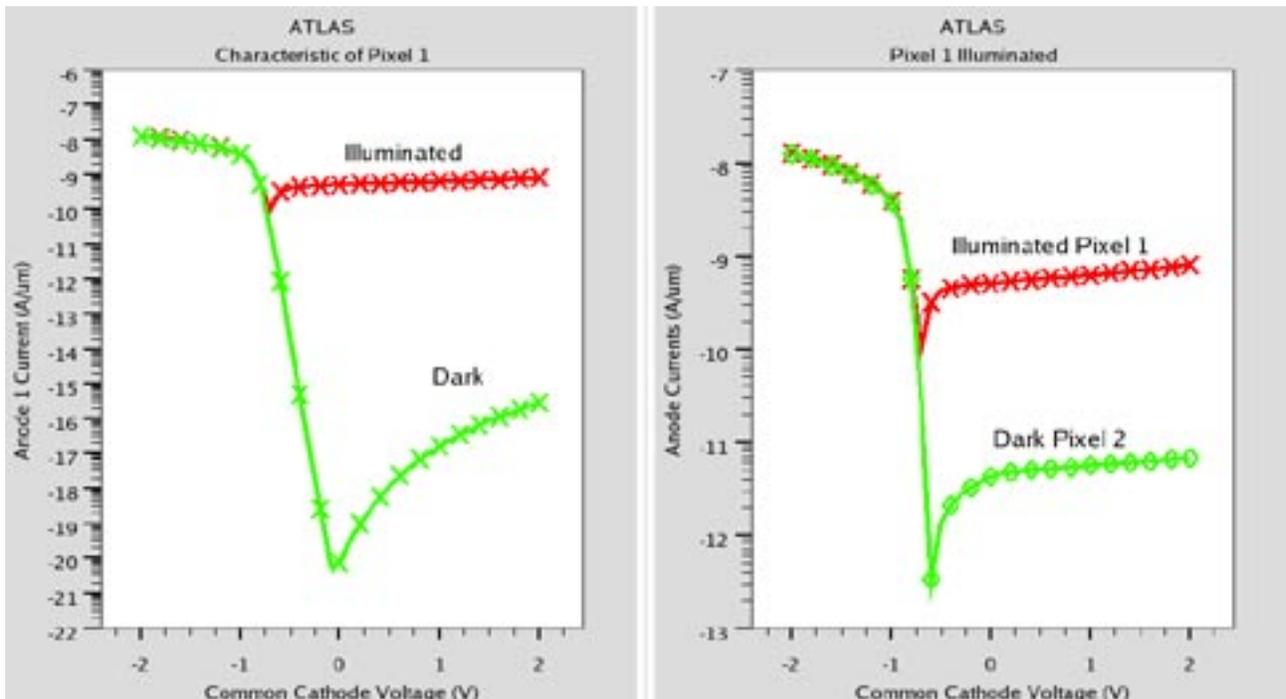


Figure 4. IV Characteristics of Pixels. Only Pixel 1 is illuminated homogeneously with light of 550 nm wavelength.

illuminated pixel 1 is compared with the current through the neighboring dark pixel. Although no bias is applied between the anodes of the two pixels, a considerably higher reverse current is observed in the dark pixel if the neighboring pixel is illuminated. This indicates, that the observed increase in current of the dark pixel originates in a laterally spread photo-voltaic effect causing internally different biases at the Schottky contact between the active and the PEDOT layer. By applying a bias between the anodes of the two pixels, a similar effect together with direct conduction along the PEDOT layer can be observed. The corresponding IV curves are shown in Figure 5. The magnitude for the current along the PEDOT layer is in the present example typically about 95% of the observed current between the pixels. This was checked by introducing a small dielectric barrier to separate the PEDOT layer between the two pixels.

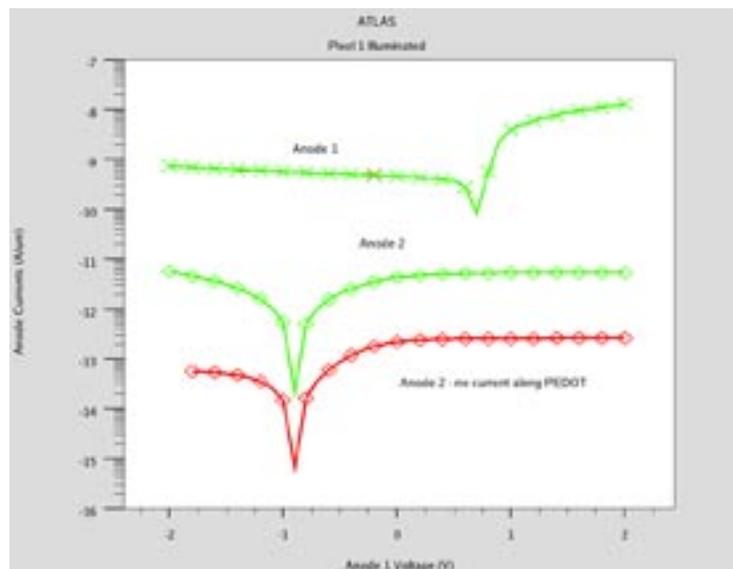


Figure 5. Anode currents for the two neighboring pixels. Pixel 1 is illuminated. The common cathode is grounded. The red curve is calculated for a device with a thin dielectric layer to separate the two pixels electrically along the PEDOT layer.

## Conclusion

Employing the models implemented in *ATLAS*, we investigated the electrical crosstalk of neighboring pixels with and without illumination. The transfer matrix method was used to calculate the light intensity profile within the given layered structure, taking into account the realistic complex refractive index of the materials. The results indicate, that the crosstalk between the given pixels is not only direct via the shorting PEDOT layer between the anodes of the pixels, but also due to the electric crosstalk along the highly conductive common bulk layer.

# Multi-layer Organic Light Emitting Diode Simulation

A conventional 2-layer organic light emitting diode consists of a hole transport layer (HTL) and an electron transport layer (ETL). A good OLED structure requires sufficient carrier injection so that a large exciton density is generated when the carriers recombine. However, a 2-layer OLED structure has a low injection current due to the poor metal/organic material interface and therefore has a low device output efficiency. The electron injection current can be increased by using a different cathode material such as LiF/Al. Unfortunately, LiF/Al metal processing is hard to control and is very sensitive to processing conditions. Also, hole injection is limited by the ITO anode which has a large metal/organic barrier.

Recent advances to higher injection current have been made possible by using a p-i-n structure[1] with high p-doping in the hole transport layer, high n-doping in the electron transport layer and a dopant-host emission layer (EML). By selecting the dopant in the EML, red, green and blue OLEDs can be made. The output efficiency can be improved by good metal/organic injection processing.

So far, organic light emitting diode simulations have been used to simulate hole-only or electron-only unipolar devices or simple 2-layer structures. These simple devices can easily be simulated and effects such as hole injection, bulk transport, and electron-hole recombination at the HTL/ETL interface can be analyzed. Commercial OLED structures are multi-layer and so it is necessary to understand the basic principles of organic/organic interfaces as well.

In this article we examine a 3-layer OLED and show why it has a higher device efficiency than 2-layer OLEDs.

## Hole Only Device

As a first step, the basic transport mechanisms are demonstrated using a simple hole-only unipolar organic device. The anode ITO transport material workfunction

		m-MTDATA	I-Naphdata	a-NPD	Alq3
$\mu_p$	$\mu_{0,RT}$	$4.79 \times 10^{-6}$	$1.18 \times 10^{-5}$	$6.1 \times 10^{-4}$	$1.86 \times 10^{-8}$
	$C_{RT}$	$3.39 \times 10^{-3}$	$2.67 \times 10^{-3}$	$1.5 \times 10^{-3}$	$3.76 \times 10^{-3}$
$\mu_n$	$\mu_{0,RT}$	$4.79 \times 10^{-8}$	$1.18 \times 10^{-7}$	$6.1 \times 10^{-6}$	$1.86 \times 10^{-6}$
	$C_{RT}$	$3.39 \times 10^{-3}$	$2.67 \times 10^{-3}$	$1.5 \times 10^{-3}$	$3.76 \times 10^{-3}$

Table 1. Parameters for field dependent hole and electron mobilities  $\mu_p$  and  $\mu_n$  (partly estimated) in m-MTDATA, i-Naphdata, a-NPD, and Alq<sub>3</sub> used for simulation. The parameters  $\mu_{0,RT}$  and  $C_{RT}$  from Eq. (44) are given in cm<sup>2</sup>/Vs and (cm/V)<sup>1/2</sup>, respectively.

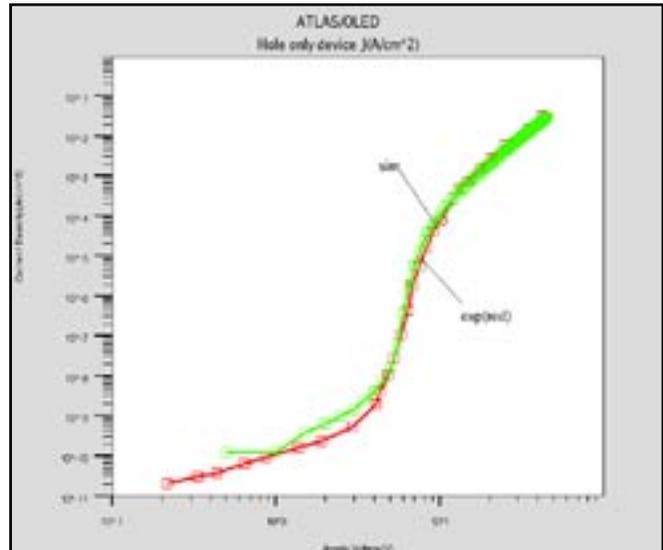


Figure 1. injection current density of hole only device

is 4.8eV and cathode metals such as Ca, Ag and Au are frequently used to inject holes. For the correct anode Schottky tunneling injection and barrier lowering, the following statements are used:

```
contact name=anode workfunction=4.8
surf.rec barrier
contact name=cathode workfunction=4.2
surf.rec barrier
```

The Schottky tunneling thermionic emission model is the key to explaining the metal/organic interface injection mechanism. The zero-field injection barrier,  $\phi_B$  can be extracted from the y-axis intercept plot of  $\log(j_{RS})$  vs.  $F^{1/2}$ , where  $j_{RS}$  is defined as:

$$j_{RS} = A \cdot T_2 \cdot \exp\left(\frac{-\phi_B + \beta_{RS} \cdot \sqrt{F}}{k_B \cdot T}\right), \quad \beta_{RS} = \sqrt{q^3 / 4\pi\epsilon_0}$$

$$A = 4q^2 m^* k_B^2 / h^3 (= 120 A / (cm^2 K^2))$$

The organic layer mobility  $\mu_n$  and  $\mu_p$  and the critical field value are listed in Table 1 [2]. The LUMO is set to 2.3eV and the HOMO set to 5.0eV. Ag is used for the cathode metal to block electron injection. The Poole-Frenkel (PF-MOB) model is used for field-dependent mobility:

$$\mu_n(E) = \mu_{0n} \cdot \exp\left(\sqrt{\frac{E}{E_{0n}}}\right)$$

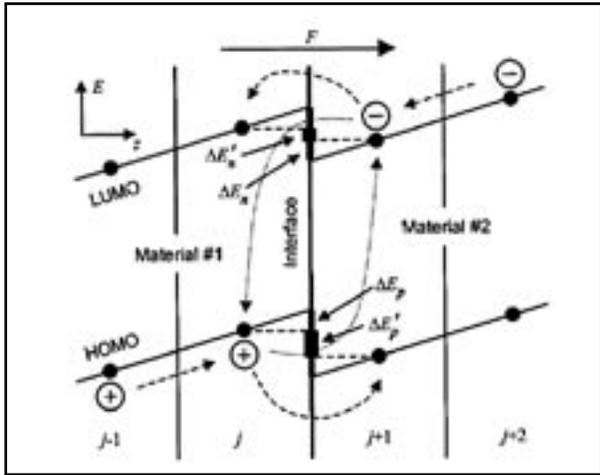


Figure 2. Interface barrier reducing by interface DOS

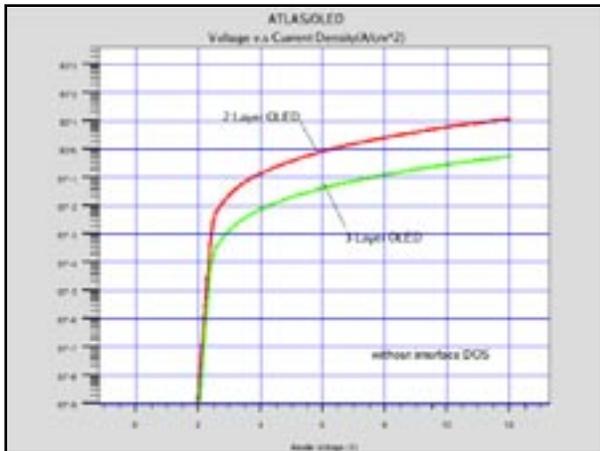
The bulk traps in the organic material are taken into consideration by a deep trap density of  $1.9 \times 10^{16} \text{ cm}^{-3}$  at a trap depth of 0.7eV. For these traps, an exponential decay function can be used to simulate the appropriate DOS distribution:

$$g_A(E) = \frac{h_0}{k \cdot T_{ca}} \exp\left(\frac{E - E_c}{k \cdot T_{ca}}\right)$$

However, a more general model can also be used to account for guest-host doping systems. This uses two Gaussian distribution functions rather than the simpler non-degeneracy trap state:

$$g_A(E) = \frac{N_{tr}}{\sqrt{2\pi}\sigma} \exp\left(-\frac{(E - E_c)^2}{2\sigma^2}\right) + \frac{N_{tr}}{\sqrt{2\pi}\sigma} \exp\left(-\frac{(E - E_c + E_a)^2}{2\sigma^2}\right)$$

Figure 1 shows the comparison between simulated and experimental injection characteristics. Both the ohmic region and the space charge limited conduction (SCLC) region can clearly be seen.



## Multi-layer OLED

To demonstrate why the 3-layer OLED has a higher efficiency than a 2-layer device we need to understand interfacial effects. The bulk and metal/organic interfaces can be simulated using the above approach, however organic/organic interfaces require a different approach.

The main effect of the organic/organic interface is to add trap states which reduces the energy barrier height and enhance interface barrier injection. We used a Gaussian form for the interface trap states:

$$\Gamma(E) = \frac{N_{HOMO}}{\sigma \sqrt{2\pi}} \cdot \exp\left(-\frac{E^2}{2\sigma^2}\right)$$

Here,  $N_{HOMO}$  is the effective density of states in the HOMO level and  $\alpha$  is the DOS width.

According to [2], holes must overcome the barrier height of two adjacent HOMO steps to enter the EML region and either cross the interface or directly recombine with an electron. The incorporation of the interface states lowers the barrier height and so increases the probability of a charge carrier crossing the interface. Figure 2 illustrates this principle.

Figure 3 shows the IV and VL (voltage vs. luminance) characteristics without the interface states. The 3-layer OLED has a smaller injection current and the similar output luminance when compared to the 2-layer device. The luminance in  $\text{cd/m}^2$  is calculated by:

$$L = \eta_{\text{coupling}} \cdot k_m \cdot S \cdot h\nu \cdot \frac{1}{\pi}$$

where  $S$  is the integrated exciton density,  $k_m$  is  $683 \text{ lm/W}$  and the coupling value ( $\eta_{\text{coupling}}$ ) can be calculated either by ray-tracing or the transfer matrix method.

Figure 4 shows the IV and VL characteristics with the interface states at the HTL/EML interface. The device efficiency and luminance have increased.

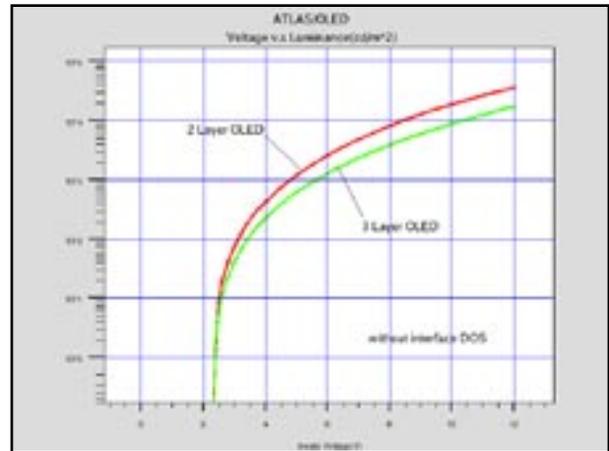


Figure 3. IV and VL without interface states.

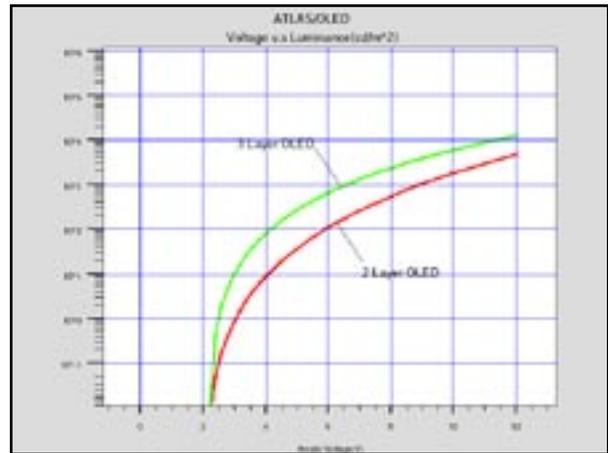
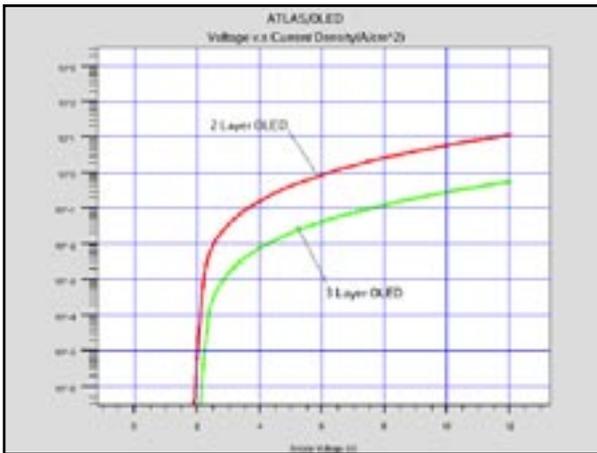


Figure 4. IV and VL without interface states.

Figure 5 shows the Langevin recombination rate and the singlet exciton density for the 2-layer and 3-layer OLEDs. The interface states in the HTL/EML interface result in a lower energy barrier. This increases the hole density at the interface and in turn increases the exciton density for the 3-layer device.

### Summary

The 3-layer OLED structure has more output efficiency than 2-layer case. This is because the HTL/EML interface has interface states which lower the energy barrier. This results in increased hole density and so exciton density. Despite the fact that the injection is lower than in the

2-layer device, the 3-layer OLED has a higher output luminance. If another injection technique, such as a p-i-n OLED, is used then multi-layer OLED will show lower operational voltage and good output efficiency.

### References

- [1]. Weiyang Gao et al, Journal of Applied Physics, vol 94, number 1, 1 July 2003.
- [2]. J. Staudigel et al, "A quantitative numerical model of multilayer vapor-deposited organic light emitting diodes", Journal of Applied Physics vol 86, Number 7, 1 October 1999.

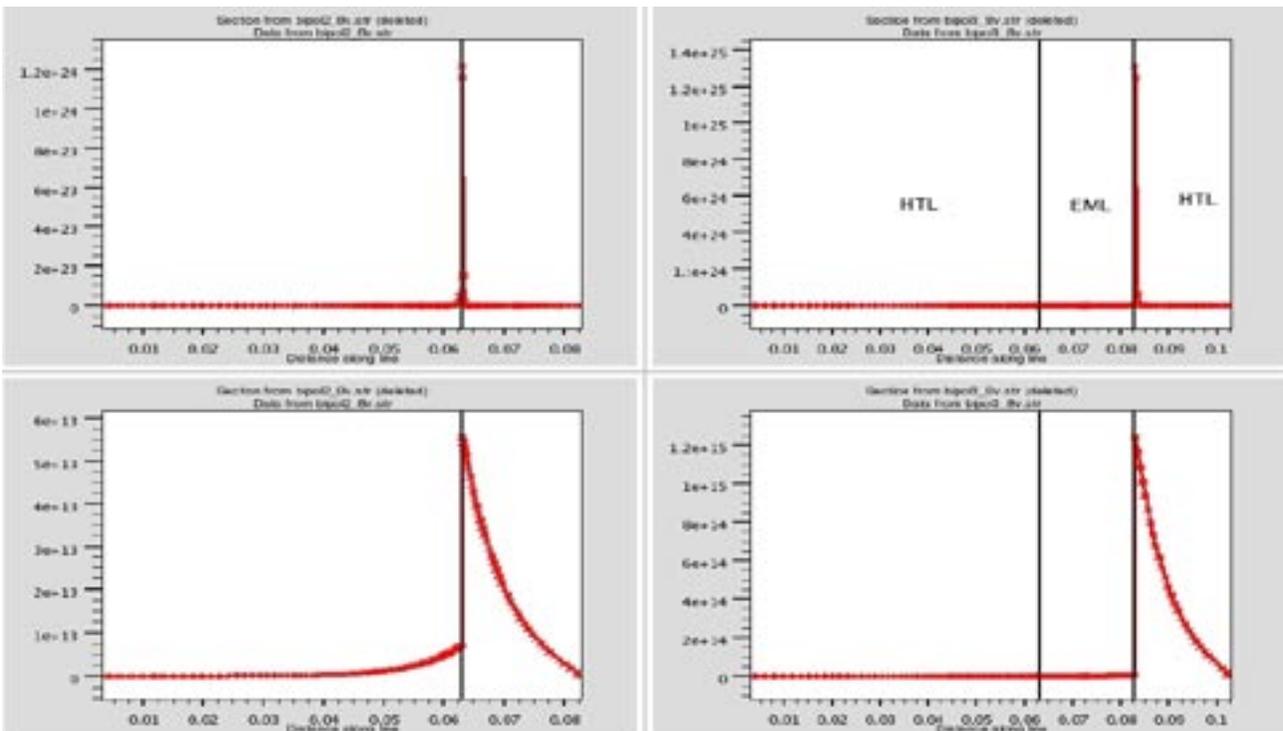


Figure 5. Langevin Recombination (top) and Singlet Exciton Density (bottom) for a 2-layer OLED (left) and a 3-layer OLED (right).

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