Simulation Standard

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Simulation of Single-Event Effects in FinFETs Using the *ATLAS 3D* Device Simulator

Introduction

A great deal of recent industry attention has focused on the use of non-planar multi-gate device structures in future generation MOS devices that feature channel lengths below about 50 nm [1-3]. The devices are based upon silicon-on-insulator (SOI) substrates, and employ three-dimensional (3D) structures that achieve fully depleted operation with near-ideal, sub-threshold slopes. Like their single-gate planar counterparts, these new SOI devices contain isolated channel regions. The transient charge injection from ionizing radiation events, including so-called "single events," can change the body potential of SOI MOSFETS and initiate transient transistor action [4-5]. This article illustrates the use of ***ATLAS 3D*** Device simulations to examine the impact of charge injection in these highly scaled 3D device structures.

Device Structure

Fully depleted SOI devices have long been of interest. However, the scalability of the single-gate devices have so far been limited by silicon thickness control, as well as the need for ultra thin silicon and/or buried oxides. Double gate devices, which have a gate on both the top and the bottom of the channel, often overcome these limitations [6], but process integration issues limit the practical implementation of devices with high transistor densities. Two proposed 3D-device structures are each a variation of the double gate device: the FinFET essentially turns the double gate device on its side [1], while the tri-gate device uses a thin gate oxide on three sides of the device, instead of on only two [2]. Both devices use elevated (thicker) source and drain regions, and is contain electrically floating body regions. Figure 1 illustrates the device structure.

Device Simulation

In a laboratory simulation, ***ATLAS 3D*** Device was used to simulate the impact of single-event charge injection into various regions of a FinFET device. Figure 2 is the simulated device structure as viewed with ***TonyPlot 3D*** and ***TonyPlot 2D***. The starting point was the device published by Huang, et al [1]. Device parameters were calibrated based on published physical dimensions with other parameters set to best match the published DC current values for the PMOS device. Appropriate changes were then made in order to create the NMOS device used in these simulations. The drain and source doping is N+ ($1x10^{19}$ cm^{-3}) and that of the body is P- ($1x10^{16}$ cm^{-3}). The gate workfunction was set to 4.6 eV in order to achieve a reasonable threshold voltage of about 0.2 volts [7, 8]. The subthreshold DC - IV characteristics (Figure 3) indicate a slope of 64 mV/decade.

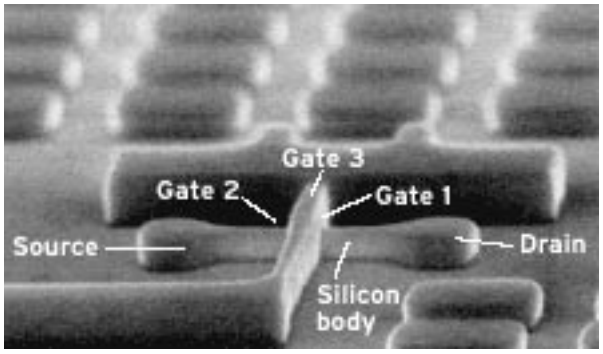

Figure 1. 3D device structure such as used for the FinFET [1] and Tri-Gate [2] devices. Figure from [3]. *(COPYRIGHT IEEE Spectrum)*.

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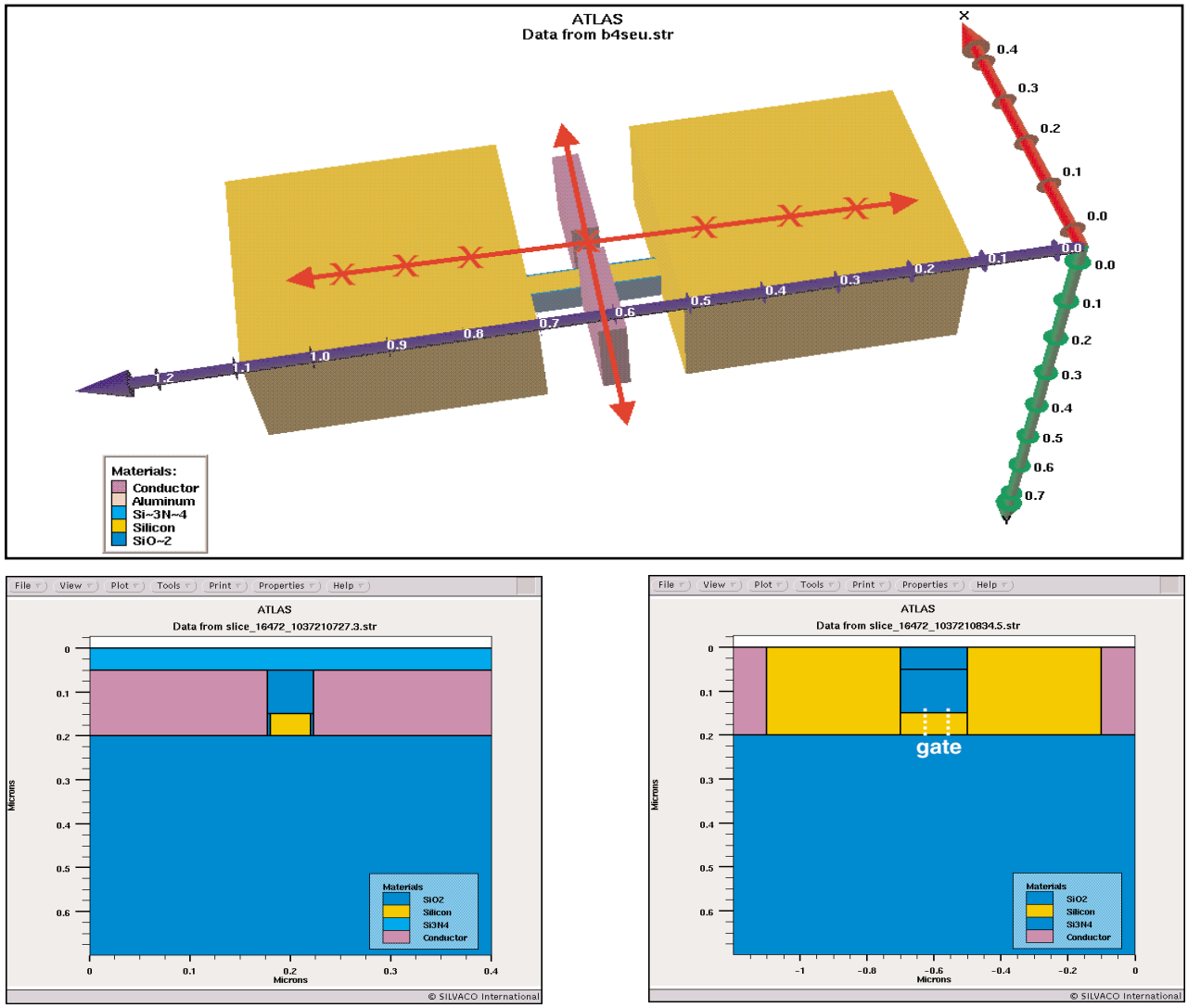

Figure 2. Simulated FinFET device. Top: 3D view with some layers not shown. The arrows show the cross section locations, the "X" 's show approximate locations for simulated "hits". Bottom left – cross section along the gate; bottom right – cross section along the channel from drain to source.

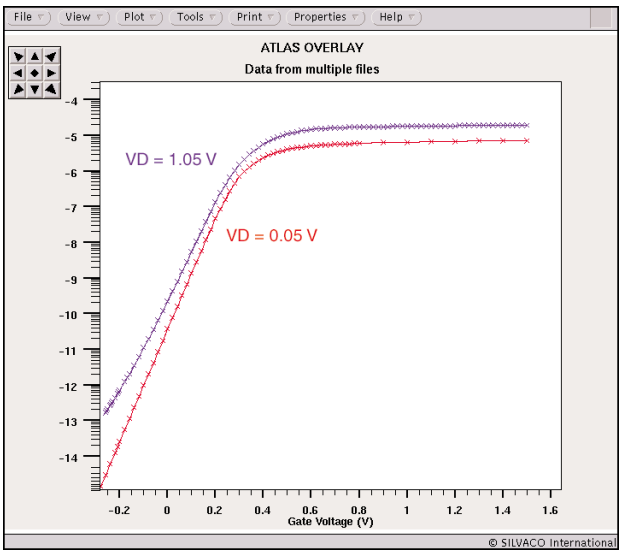

Figure 3. Simulated DC IV curves for the NMOS device. The subthreshold slope is 64 mV/decade.

The charge (electron-hole pair) generation is defined using the singleeventupset statement of ***ATLAS 3D*** Device [9]. The statement used for these simulations is (where the z-value of the entry and exit coordinates were varied for the different hit locations):

```
singleeventupset entry="0.1,0.0,0.2" \
  exit="0.1,0.05,0.2" radius=0.05 \
  density=1.e18 t0=4.e-12 tc=2.e-12
```

Two things worth noting:

(1) the scale of the pulse's temporal profile is on the order of the carrier, which is the transit time across a biased junction (i.e. ~ 10 ps)

(2) the spatial profile of this pulse would cause truncations of the generation region by the device active region physical limits in the body, as well as in some portions of the drain / source regions

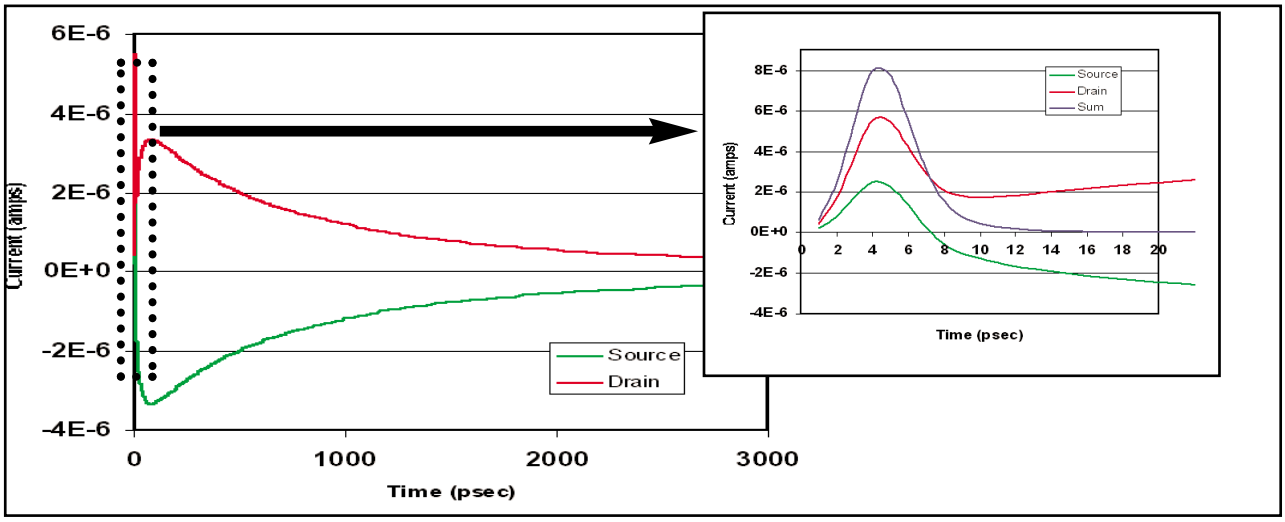

Figure 4. Drain and source currents for the hit to the body region. The insert shows a zoomed-in view of the initial time response due to the injected charge.

Simulation Results

The FinFET device was biased with the drain voltage at 1.5V, and the gate and source voltages at 0V. In each case, a simulation was performed at various locations for the center of the charge injection track, perpendicular to the wafer surface. The axis of the hit location was simulated for the center of the body region, and for three locations in each in the drain and source regions. (Denoted by the X's in Figure 2, top).

Case 1:Body Hit

After injection into the body region, a fast pulse is first observed in both the drain and source current (Figure 4). This represents the excess electrons created in the body as they cross the body-drain and body-source junction. The net-induced photocurrent is represented by the sum of the two current pulses (also plotted). Excess holes trapped in the potential well of the n-p-n structure raise the potential of the body region causing the body-source junction to become forward biased (Figure 5) and initiating transistor action. This accounts for the second, longer pulse in Figure 4. While the peak value of the second pulse is less than the first, the characteristic time scale is much longer (nanoseconds compared to picoseconds), and the associated charge (integral of the current) is greater than 50 times that of the initially deposited charge.

Case 2: Drain and Source Hits

Generally for planar single-gate SOI devices of past and current generation devices (≥ 0.13 um), injection into the body is believed to result in the most pronounced device response since it most efficiently initiates parasitic bipolar action. There has been some discussion about hits to the drain region also contributing [10] to device response. In the present simulated devices, the dimensions of the drain and source regions are comparable to the radial dimensions of the simulated charge track. Simulations were performed with the center of the track at three different locations within the drain and within the source relative to the body silicon region: at 0.3 um, 0.2 um, and 0.1 um away from the thin body region edge (Figure 2, top). The resulting drain currents for each case are plotted in Figure 6. The same trends are observed for both drain and source with the collection efficiency being somewhat less on the source side due to the lower junction bias.

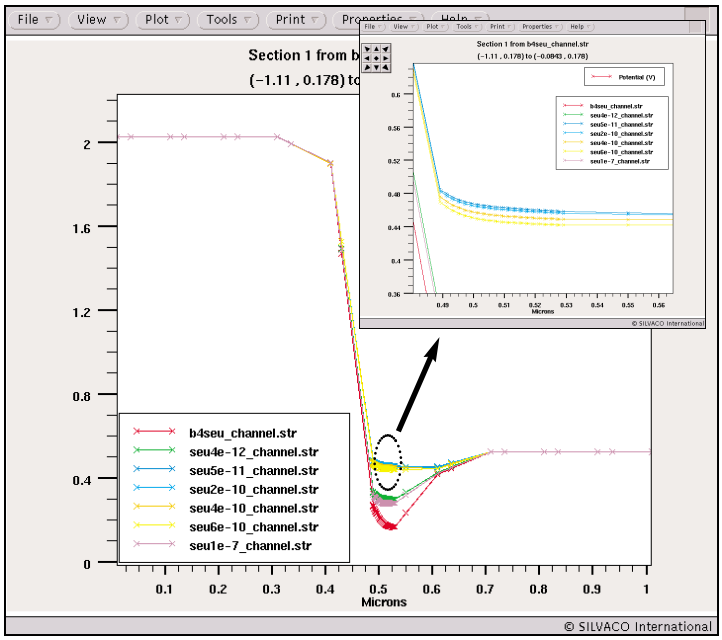

Figure 5. Potential distribution – evolution over time showing the body potential increase due to the charge injection. Plots are shown at times: pre-strike (b4), 4ps, 50ps, 200ps, 400ps, 600ps, and 0.1us.

In both cases, some holes generated in the drain (source) region are able to drift and diffuse to the body junction. The initial fast rise is carriers that are in and near the high field region of the junction, while the longer tale is dominated by diffusion to the junction. For a doping of $10^{19}cm^{-2}$ in the drain, the minority carrier lifetime is on the order of 50 ps, and the diffusion length on the order of 0.35 um. It is for this reason that the initial current decreases as the hit location is moved away from the drain-body junctions from 0.1 um to 0.3 um.

Comparing the results from the drain/source regions (Figure 6, left) to that of the body (Figure 4), the former produces a comparable (or larger) device response. This is due to the small device dimensions compared to carrier diffusion lengths (allowing charge collection), and the larger volume of the drain/source silicon leading to increased volume for charge generation to drive the bipolar action.

Conclusion

ATLAS 3D Device simulations are used to simulate the impact of single event charge injection into a sub-50nm FinFET device. Simulation results indicated that the injected charge is amplified by transient transistor action, and that the sensitive areas of such devices may include source and drain regions.

References

[1] X Huang et. al., "Sub 50-nm FinFET:PMOS", IEDM Technical Digest, 1999.

[2] R. Chau et. al., Advanced Depleted-Substrate Transistors: Single-Gate, Double-Gate, and Tri-Gate", 2002 International Conference on Solid State Devices and Materials (SSDM 2002), Nagoya, Japan.

[3] Linda Geppert, "Triple Gate, Double Play", IEEE Spectrum, November 1, 2002.

[4] G. E. Davis et. al, "Transient Radiation Effects in SOI Memories, IEEE Transactions on Nuclear Science, vol. NS-32, pp. 4432-4437, December 1985.

[5] M. Alles, "SPICE Analysis of the SEU Sensitivity of a Fully Depleted SOI CMOS SRAM Cell, IEEE Transactions of Nuclear Science, vol. NS-41, pp. 2093-2097, December 1994.

[6] J.-P. Colinge ed., Silicon-on-Insulator Technology: Materials to VLSI, Kluwer Academic Publishers, pp. 169, 1991.

[7] J. Kedzierski et al., "Metal-gate FinFET and fully-depleted SOI devices using total gate silicidation", IEDM Technical Digest, pp. 247-250, December 2002.

[8] Y.-K. Choi et al., "FinFET Process Refinements for Improved Mobility and Gate Function Engineering", IEDM Technical Digest, pp. 259-262, December 2002.

[9] Atlas Users Manual, Volume II, Silvaco International, 2001.

[10] P. Dodd et. al., "SEU-Sensitive Volumes in Bulk and SOI SRAMs From First-Principles Calculations and Experiments", IEEE Transactions of Nuclear Science, pp. 1893-1903, December 2001.

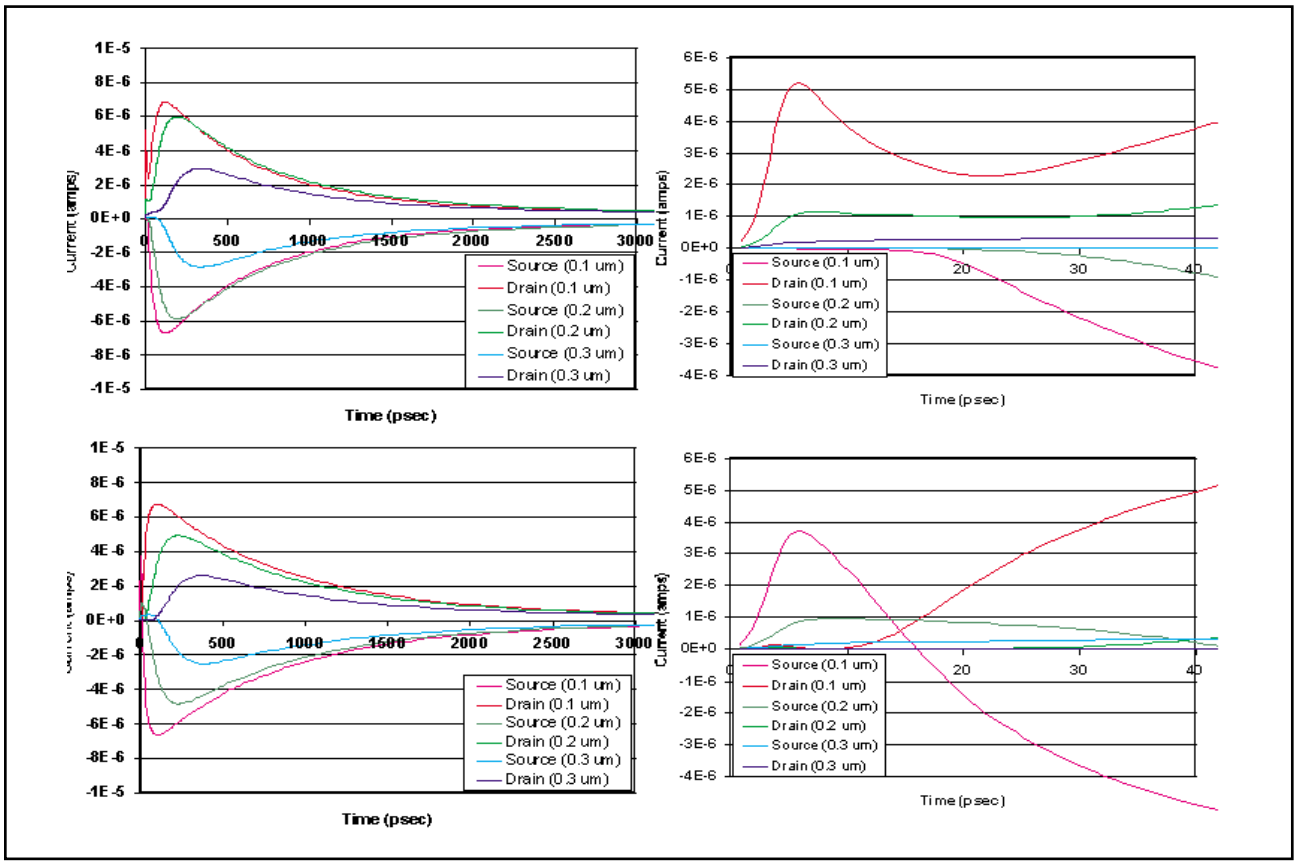

Figure 6. Drain and source currents for the hit to the drain region (top) and source (bottom) at three locations. Figures on the right show initial 40 picoseconds.

Simulation of a Double Ridge Edge Emitting InGaAsP/InP MQW Laser

Introduction

In order to investigate the influence of ridge separation on the transverse optical modes of a double ridge edge multiple quantum well (MQW) emitting laser, we have designed a generic device based on the InGaAsP/InP MQW 1.5µm wavelength emission. The aim of this study is to investigate power loading in the structure with increasing bias using the bottom layer as the reference plane.

To do this, the first three transverse modes were considered and the power associated with each mode was monitored as a function of the device design. Silvaco ***ATLAS LASER*** was used for this investigation.

Active Region

The active region of the chosen device was based on a publication by J. H. Song, et al. that appears in IEEE Photonics Technology Letters, Vol12, 7 July 2000. The Multiple Quantum Well region was specified with the MQW statement. The XMIN, XMAX, YMIN, and YMAX parameters define this region. The width of each well is defined by the (WW) parameter, the well separation is defined by the (WB) parameter, and the number of wells used is defined by the (NWELL) parameter.

Schrodinger's Equation is performed to extract bound state energies. The NX and NY parameters specify the quantum mesh that is required for the solution of Schrodinger's Equation. This will define a box of uniform mesh within the MQW region. We have also specified the YAN model in order to calculate the spontaneous recombination from a hole band.

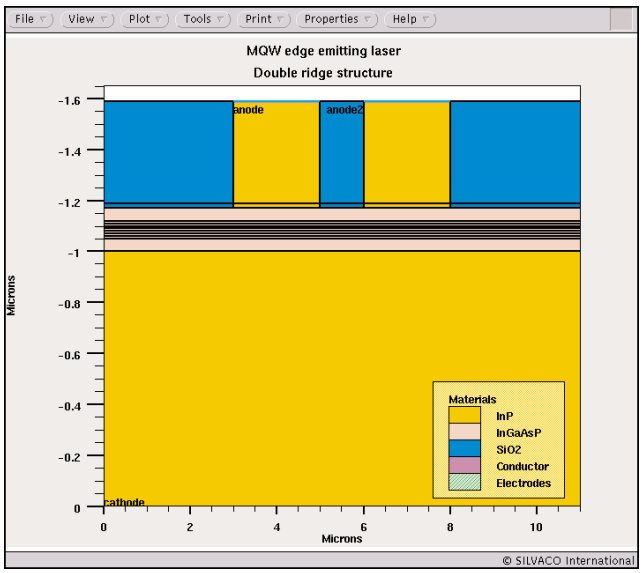

Figure1. the structure of the two laser devices used for this study. Note the laser ridges and their separation.

In order to take account of the strain in the MQW system, the Ishikawa model was invoked. The band edge parameter is modified for Schrodinger's Equation by defining the strain percentage. There are a number of tabulated, user-definable factors that modify the effect of the strain on the conduction and valance-band effective masses. These are found in Ishikawa's paper (Takuya Ishikawa and J.E. Brown, IEEE Journal of Quantum Electronics, Vol 30, No 2, Feb 1994 pp 562-570) and are reproduced in the *ATLAS User*'s manual (Quantum chapter).

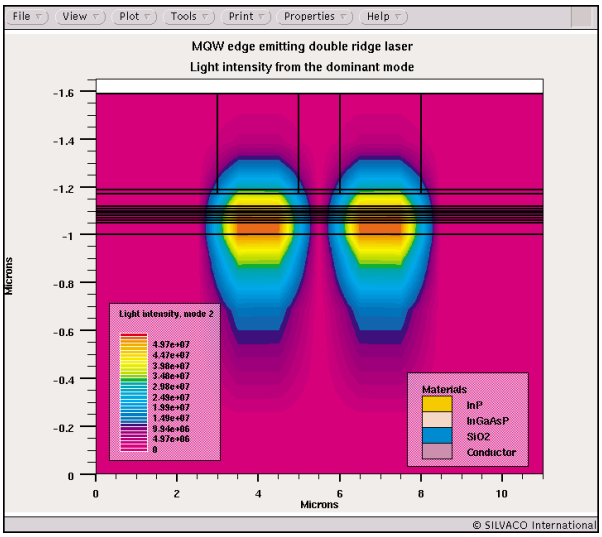

Figure 2a. Light intensity contour map from the dominant transverse mode in a structure with 1µm separation.

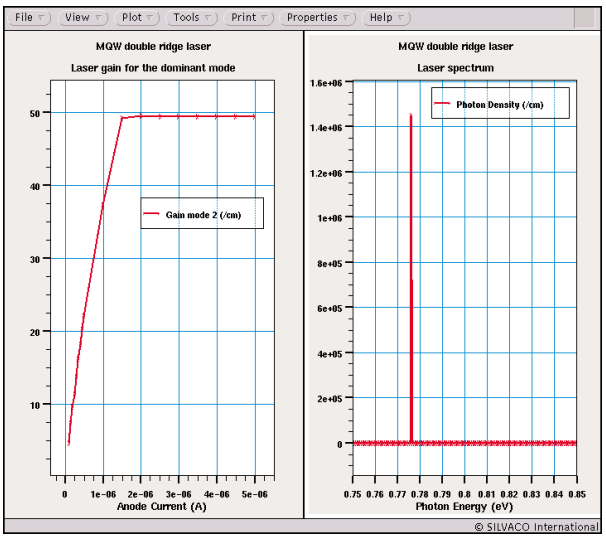

Figure2b. Laser gain and frequency spectrum for the 1µm structure at an anode current of 1e-5A.

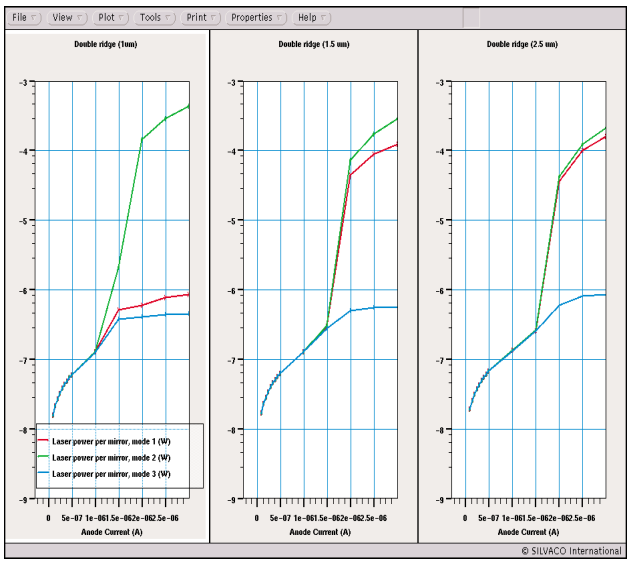

Figure 3. Laser power output from Three structures with ridge separation of 1 micron (left panel), 1.5 micron (middle panel) and .5 micron (right panel).

The materials used in this example were defined in the usual way: molar fractions were specified in the region statements, while the quantum wells molar fractions were defined in the MQW statement.

The Laser Structure

The structure was defined using the region statements in which several parameters were specified, including thickness, y mesh density, x position, material concentration, and doping concentration. This simplifies the definition of the y mesh point as the regions are stacked on top of each other. Here in order to define the five laterally stacked regions (oxide/ridge/oxide/ridge/oxide) the parameter STAY was utilized within the region statement (Figure 1).

Figure 2a shows a map of the light intensity for the dominant lateral mode of a structure with a 1um ridge separation at a current of 1e-5A. Figure 2b shows the laser gain and frequency spectrum under the same structure and bias conditions.

The Experiment

In order to obtain a structure with a single transverse mode, laser simulations were run with the first three principle transverse modes taken into account, up to a current of 1e-5A. The modes were monitored as a function of the ridge separation(s). For this work, the ridge width (r) was kept at a constant 2mm. In order to simplify this investigation, we used fixed statements for separation and other dimensions with algebraic expressions. These were defined in the beginning of the input deck in order to simplify the generation of data for various device dimensions.

Influence of the ridge separation on the modal laser power:

The results in Figure 3 show the output laser power as a function of current flowing through the structure. The results from the first three transverse modes show that when the ridge separation exceeds 1 micron, the laser shows a bi-modal operation, with the power of the first two modes being fairly similar. Under bias conditions where the anode current is 3e-6A, the first two modes are within the same order of magnitude. As the separation reduces to 1 micron, the laser operates with one dominant mode that generates power about 3 orders of magnitude greater than the other two modes at a bias of 3e-6A anode current.

Temperature Distribution in the Device

Figure 4 illustrates a 2D map of the lattice temperature contours in a device with a 2µm separation between the ridges. The bottom cathode plane was used as a reference temperature (300K) for these calculations. As expected, the areas of maximum temperature coincide with the active regions where most of the current passes and the recombination events take place. At a bias condition of 1e-5A anode current, the temperature rise is rather small. However, it is a good indicator of the trend in the device temperature with increasing bias.

Conclusions

In this study, we demonstrated the use of ***ATLAS LASER*** to fine-tune the design of a multiple quantum well (MQW) edge-emitting laser. For this typical 1.5µm wavelength InGaAsP/InP laser, the separation between the two light confining ridges must measure around 1µm to ensure a single mode operation.

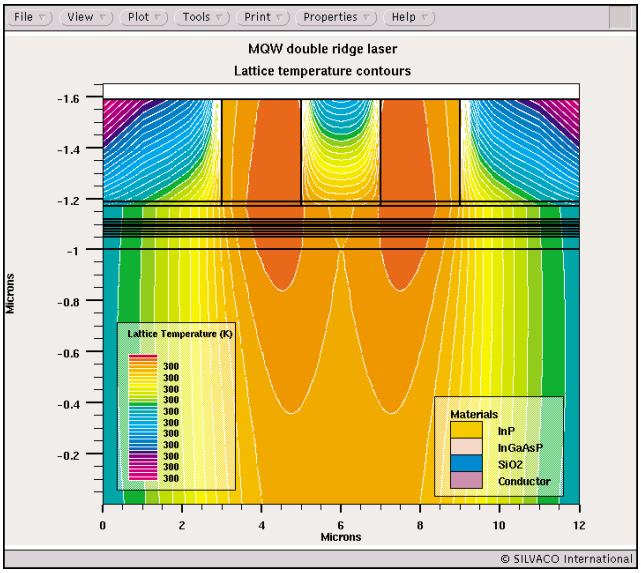

Figure 4 showing a typical lattice temperature contours in a device with 2mm ridge separation. Note the areas with maximum temperature coincide with areas of maximum lasing activity.

Quantum Modeling, Part I : Poisson-Schrodinger Solver

1. Introduction

The trend toward smaller MOSFET devices with thinner gate oxide and greater doping is resulting in the increased importance of quantum mechanical effects, which are observed as shifts in threshold voltage and gate capacitance. Predicting these quantum effects requires solving the Schrodinger equation. This article (part 1 of a series) presents the Poisson-Schrodinger solver and its enhancements implemented in ***ATLAS*** from Silvaco. Section 2 presents the syntax used to perform the simulation. Section 3 presents the MOS-capacitor simulation results and compares them with results obtained with the University of Pisa code [1-6].

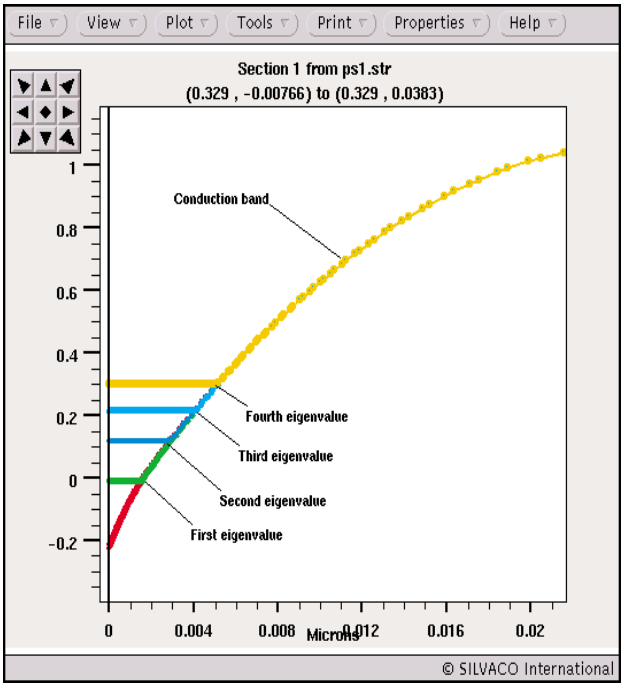

Figure 1. The first 4 eigenvalues for the electron longitudinal effective mass and the conduction band (in eV).

2. Poisson-Schrodinger Solver in ATLAS

To consistently solve Poisson and Schrodinger equations with ***ATLAS***, the user must specify different parameters in the MODELS statement:

```
models fermi schro new.eig ox.poisson \
qy.min=<val> qy.max=<val> \
qx.min=<val> qx.max=<val> \
ox.schro fixed.fermi
```

`fermi` specifies the Fermi-Dirac statistics, `schro` sets the Schrodinger solver for electrons, `ox.poisson` specifies the oxide to be considered as a semiconductor, `new.eig` specifies the new eigensolver, `ox.schro` indicates that the silicon oxide is included in the Schrodinger domain, (`qx.min`, `qx.max`, `qy.min`, `qy.max`) define a box where the Schrodinger equation is solved, `fixed.fermi` sets the quasi-fermi levels to zero, `disp` sets the type of eigenvalues/vectors to display. The new parameters `new.eig`, `ox.poisson` `qx.min`, `qx.max`, `qy.min`, `qy.max`, `ox.schro` are explained below.

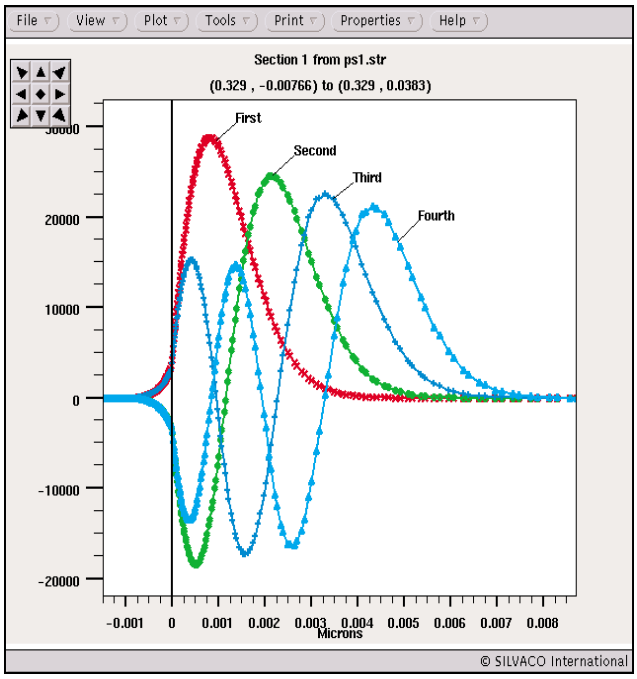

Figure 2. The first 4 eigenfunctions for the electron longitudinal mass near the interface oxide/silicon (in $m^{-1/2}$).

A new eigensolver is implemented in ***ATLAS*** that exhibits a better convergence and speed than the previous version. The eigenvalues finder is based on the QL-algorithm for tridiagonal matrices and the eigenvector finder based on the inverse iteration method. Since the potential at the edges of the Schrodinger domain is considered infinite and only silicon is considered, the oxide should be included in the Schrodinger domain with `ox.schro` in order to take into account the actual barrier at the oxide/silicon interface. This approach lets eigenfunctions penetrate into the oxide. The quantum box should be defined (with `qx.min`, `qx.max`, `qy.min`, `qy.max`) so that qy.min is within the oxide. Finally, the flag `ox.poisson` indicates that the charge in the oxide, like a semiconductor, is included in the Poisson equation.

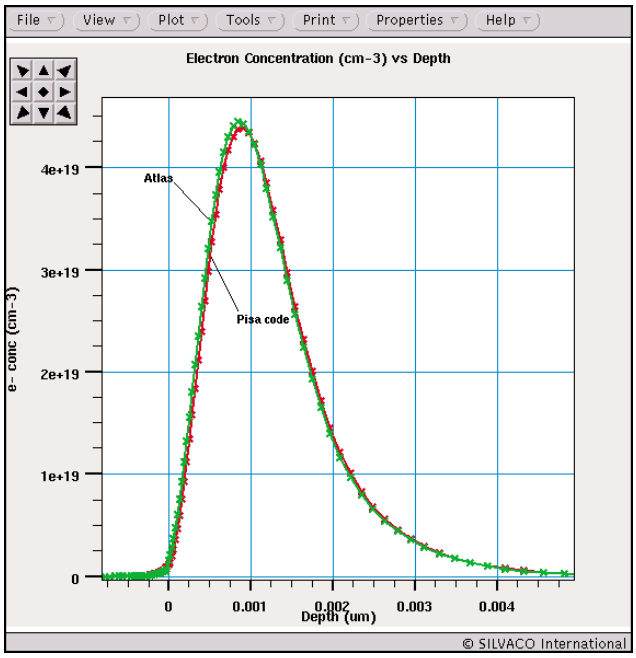

Figure 3. Electron concentration vs depth. The red curve is from the Pisa code and the green one from ***ATLAS***.

The user may now set new material parameters for the effective masses and degeneracy factor. The default values in silicon and silicon oxide are:

```
material material=silicon ml=0.98 \
   mt1=0.19 mt2=0.19 mhh=0.49 \
   mlh=0.16 degeneracy=2
material material=sio2 ml=0.3 mt1=0.3 \
   mt2=0.3 mhh=1 mlh=1 degeneracy=1
```

`ml` is the electron effective longitudinal mass, `mt1` and `mt2` are the electron transverse effective masses, `mlh` and `mhh` are the effective masses of light and heavy holes, and `degeneracy` is the degeneracy factor. The Schrodinger solver for holes and their effective masses is used when `p.schro` is set in the MODELS statement.

Finally, before applying a bias on the electrodes, the user should specify the Poisson and Schrodinger equations to solve and disable the continuity equations:

```
method carriers=0
```

3- Results

A p-type MOS-capacitor was defined in ***ATLAS***. Silicon is 2.5e18 cm^{-3} p-type doped, and the gate oxide is 1.5 nm thick. For 1V applied on the gate while in inversion mode, Figures 1 and 2 show the first 4 eigenvectors and eigenvalues related to the longitudinal effective mass. The x=0 coordinate on these figures stand for the oxide/silicon interface. Figure 2 shows the clear penetration of the eigenfunctions in the oxide.

Figure 3 displays the relatively good agreement between electron concentration (for Vgate=1V) and its comparison to the electron concentration obtained with the code of the University of Pisa. Then, in Figure 4, this electron concentration is compared with the one obtained after a semi-classical simulation. This overlay shows that the maximum of the electron concentration is beneath the interface in the quantum case and its value is smaller than the semi-classical case. This position is directly linked to the position of the maximum of the electron probability distribution given by the first eigenvector (red curve in Figure 2).

As commonly used, one can also perform C(V) curves. In ***ATLAS***, the low frequency C(V) curve can be computed in static operation: the charge concentration is integrated in the whole structure and then this quantity is derived as C=-dQ/dV. To get the charge in the ouput file the user should specify the charge parameter in the OUTPUT statement. The integrated net charge will be saved in a logfile with the help of the probe command:

```
probe name=charge charge integrate left=0.0 right=1.0 \
top=0.0 bottom=1.0
```

where (left, right, top, bottom) are the edges of the silicon region.

Then, the capacitance is computed using the EXTRACT command in ***DeckBuild***:

```
extract name="dQdV" \
deriv(v."gate", -1e-04*probe."charge") \
outfile="CV.out"
```

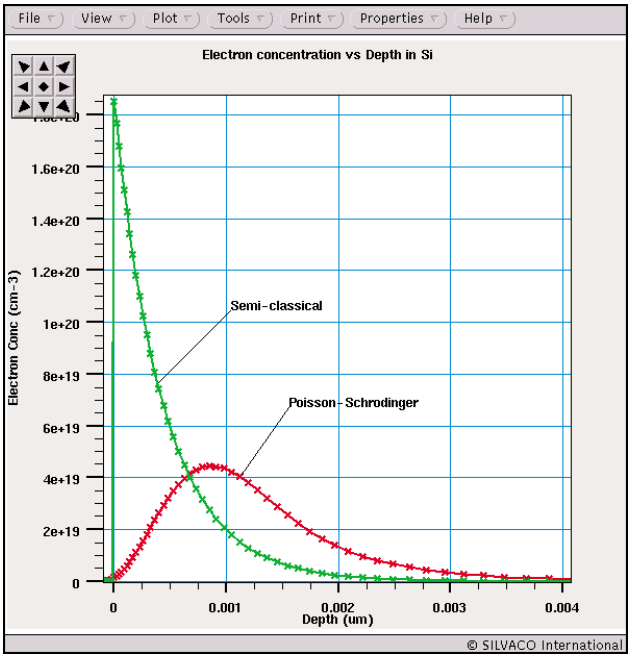

Figure 4. Electron concentration vs depth for semi-classical (green curve) and Poisson-Schrodinger (red curve) models.

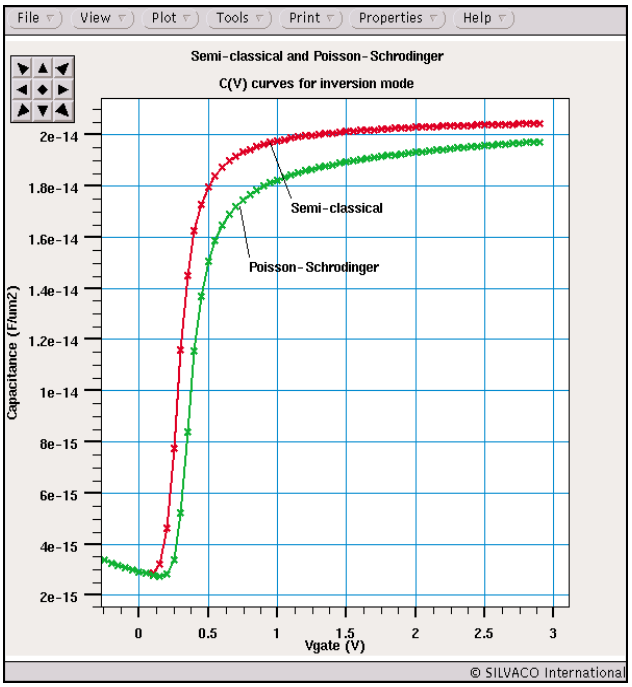

Figure 5: comparison of the semi-classical and Poisson-Schrodinger C(V) curves in inversion mode.

The 1e-04 factor gives the capacitance in $F/\mu m^2$.

Figure 5 illustrates the overlay of the semi-classical and quantum C(V) curves for the same p-type MOS-capacitor as previously described. In inversion mode, the quantum capacitance is smaller than the semi-classical capacitance; this effect is expressed like a thicker effective oxide in a quantum case, rather than the actual oxide obtained in semi-classical case. The electron depletion region beneath the interface showed in Figure 4 explains it. Figure 6 shows the good agreement obtained with an ***ATLAS*** comparison of the quantum C(V) curve and the University of Pisa code.

4- Conclusion

This paper has presented the new features of ***ATLAS*** dealing with Poisson-Schrodinger simulations, including a new eigensolver that takes into account the silicon oxide, the different effective masses, and the degeneracy factors for silicon and silicon oxide. This solver has shown good results when compared to the code of the University of Pisa. This solver extends to nonplanar structures originating in the Silvaco process simulator ***ATHENA*** by adding the `new.schro` parameter in the MODELS statement. We have shown in this paper that ***ATLAS*** now includes an accurate Poisson-Schrodinger solver. In Part II of the article this model will be used to calibrate the Density Gradient model. Part II will be presented in a future *Simulation Standard* issue.

References

[1] G.Iannaccone, M.Macucci, P.Coli, G.Curatola, G.Fiori, M.Gattobigio, M.Pala, "Towards nanotechnology computer aided design: the NANOCAD project", IEEE-NANO 2001.

[2] G.Fiori, G.Iannaccone, "The effect of quantum confinement and discrete dopants in nanoscale 50nm n-MOSFETs: a three-dimensional simulation", Nanotechnology 13 (2002) 294-298.

[3] G.Fiori, G.Iannaccone et al., "Experimental and Theoretical investigation of quantum point contacts for the validation of models for surface states", Nanotechnology 13 (2002) 299-303.

[4] G.Fiori, G.Iannaccone, "Effects of quantum Confinement and discrete dopants in nanoscale bulk-Si nMOSFET", IEEE-NANO 2001.

[5] G.Fiori, G.Iannaccone, "Modeling of ballistic nanoscale metal-oxide-semiconductor field effect transistors", Applied Physics Letters, vol.81, 19, Nov.2002.

[6] G.Iannaccone, G.Fiori, G.Curatola, "Techniques and methods for the simulation of nanoscale ballistic MOSFETs", IEEE-NANO 2002.

We thank the University of Pisa for its data and contribution to this work.

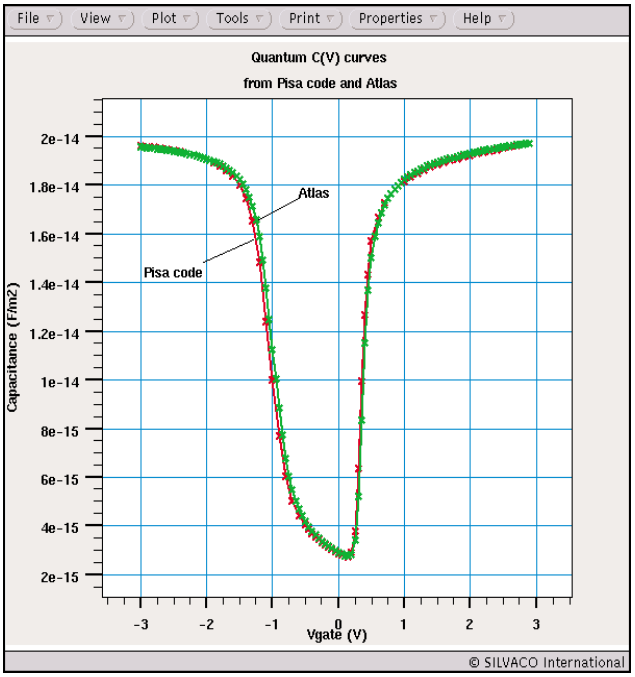

Figure 6. Comparison of the C(V) curves obtained from Pisa code (red curve) and ***ATLAS*** (green curve).

The Simulation of a High Gain InP/InGaAs/InP Double HBT with Varying Doping Profile Provided by ASCII User Defined External Files within the *ATLAS* Framework

1.0 Introduction

A PN junction is formed when a P-type doped portion of a semiconductor is joined with a N-type doped portion. The PN junction forms the basic unit of a bipolar transistor [1] and is a fundamental component for functions such as rectification. If both the P-type and the N-type regions are comprised of the same semiconductor material, the junction is called a homojunction, used for many years in the form of bi-polar junction transistors (homojunction BJTs) [1]. After many iterations and decades of development and improvement, the most innovative change is the replacement of the homojunction emitter material with larger energy gap material.

It is possible to now create new heterojunction and double heterojunction bipolar transistors [2] utilizing junction layers made of different heterojunction semiconductor materials. Typically a heterojunction bipolar transistor (HBT) consists of a hetrojunction at the base-emitter junction and a homojunction at the base-collector junction. A double hetrojunction bipolar transistor (DHBT) is made of two heterojunctions, both at the base-emitter and at base-collector junctions. These developments have lead to HBTs and DHBTs of such superior quality and performance that they are now commonplace in areas of electronic commerce.

This superior performance is due primarily to the presence of a quantum well in the base-emitter junction that arises through the use of two materials of differing band gaps. Typically, InP / In(0.53)Ga(0.47)As is used. The main purpose of the quantum well is to stop the back-injection of holes from the base into the emitter, which reduces the base current and consequently increase the current gain. The quantum well also permits the increase of base doping. This lowers the resistance encountered within the base, reduces the transit time for electrons, and increases frequency performance. Adding a second heterostructure within the base-collector region (e.g. In(0.53)Ga(0.47)As / InP) improves epitaxial relationships throughout the structural growth, resulting in an overall improvement in device performance. A device's performance is also improved by the use of a graded doping profile rather than uniform doping. This aids in controlling electric fields with concomitant depletion regions and improves overall breakdown characteristics.

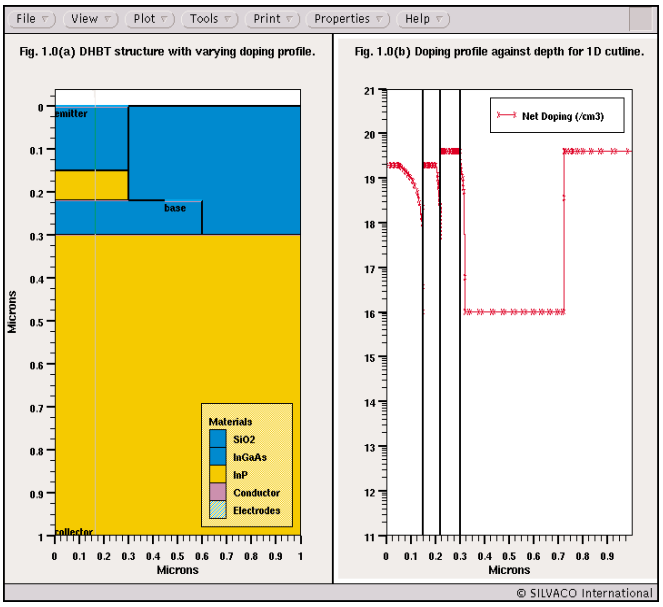

Figure 1. (a) Basic double heterostructure bipolar transistor with 1D cutline, (b) doping profile shown through 1D cutline.

2.0 Results and Discussion

In this example, a DHBT structure based on the InP / InGaAs/InP material system is simulated using Silvaco Atlas (Figure 1a). The DHBT is electrically tested, and the properties that characterize the device's DC and high-frequency performance are calculated and presented. The DC performance is shown as a Gummel plot and the DC current gain through the functions property is calculated with ***TonyPlot***. The transistor is connected in common-emitter configuration for this calculation.

The AC performance is evaluated via the cutoff frequency, ft, and the maximum oscillation frequency, fmax. The cutoff frequency is defined as the frequency at which the magnitude of AC current gain (h21) decreases to unity. The maximum oscillation frequency, fmax, is the frequency at which the unilateral power gain of the transistor tends to unity. The unilateral power gain effectively represents the maximum power gain that is achievable by the transistor. These properties are improvable with the appropriate use of heterostructures, stoichiometry, and doping in order to lower collective resistance, epitaxial strain, and other properties. These properties are incorporated within HBTs and DHBTs and offer superior performance to BJTs.

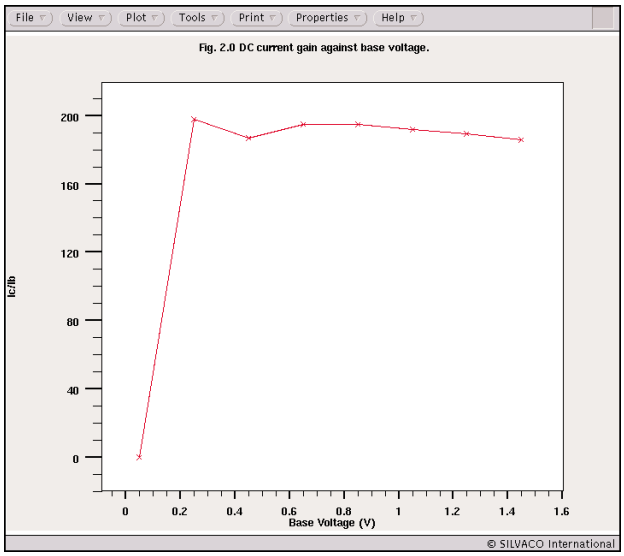

Figure 2. Simulated DC current gain versus base voltage.

This example also demonstrates the import of doping profiles previously specified in an ASCII text editor. These files are called upon during the simulation stage and the doping profiles are replicated accordingly. In this example, the files used are hbtex08_n and hbtex08_p for N-type and P-type doping, respectively. The user simply creates an ASCII text file containing two columns. The left column specifies the depth location and the right column specifies the concentration at that location.

An example would be:

```
0.0     1e16
1.0     1e20
1.001   0.0
2.0     0.0
```

```
<Must put a carriage return here>
```

ASCII text file contain no metadata and require a carriage return at the end of the file. These commands make use of the ASCII file:

```
doping <specify type> ascii infile=<filename>
```

Interpolation is used between specified the locations. Consequently, the doping profile must be set to zero at certain locations if so desired. If they are not, an interpolated value is used until the end of the device is encountered. For this example, complicated doping profiles are used throughout the structure (Figure 1b). The profile should match with the 1D cutline in Figure 1a.

The input deck is written in the Silvaco's ***DeckBuild*** environment in order to simulate the device and to evaluate its performance using specific commands. In this example, the commands:

```
doping x.min=0.0 x.max=1.0 y.min=0.0 y.max=1.0
n.type ascii infile=hbtex08_n

doping x.min=0.0 x.max=1.0 y.min=0.0 y.max=1.0
p.type ascii infile=hbtex08_p
```

invoke ASCII files previously written to specify the doping profiles. A correct h21 calculation is dependent on the careful consideration of device connections. This is achieved with the inport and outport commands, and then through solving for electrode voltages.

```
log outf=hbtex08_freq.log gains inport=base
outport=collector width=50

solve v2=1.0 v3=1.0 vstep=0.025 electrode=23
ac freq=1e7.
```

In this example, electrode 2 is the base and electrode 3 is the collector. The current gain is calculated from the ratio of Ic/Ib at DC and is designed to have a value in excess of 100 (Figure 2). The high frequency performance is satisfactory with operating frequencies in excess of 1e9Hz and gives reasonable ft and fmax as shown in Figures 3a and 3b, respectively.

3.0 Conclusions

In this report, a high gain double heterojunction bipolar transistor (DHBT) is simulated and evaluated using ***ATLAS***. It demonstrates that satisfactory results are easily achieved and specifies complicated doping profiles. These profiles are defined by the user with ASCII text files and are invoked during runtime to achieve desired effects on the electrical characteristics.

References

[1] Shockley W., 'The theory of p-n junctions in semiconductors and p-n junction transistors", Bell Syst. Tech., J., Vol 28, p435 (1949).

[2] Shockley W., U.S. Patent 2, 569, 347 (1951).

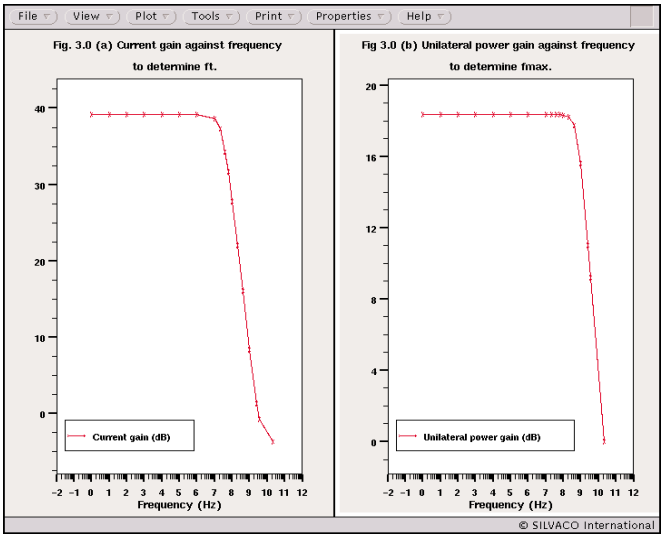

Figure 3. (a) Current gain against frequency. (b) Unilateral power gain against frequency.

Calendar of Events

November

1 LCD/PDP 2002 - Japan
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10 ICCAD - San Jose, CA
LEOS Annual Meeting-Scotland
11 ICCAD - San Jose, CA
LEOS Annual Meeting-Scotland
CS-MAX - San Jose, CA
12 ICCAD - San Jose, CA
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Hints, Tips and Solutions

William French, Applications and Support Manager

Q. If there are multiple implants in my process does the order of these implants have an influence on the result ?

A. Yes. When an implant occurs there will be some level of damage to the crystal structure of the silicon. If this damage is not annealed out then any subsequent implant will have a different penetration depth compared with the crystal that has no damage. The reason this occurs is due to the crystallographic nature of silicon. This means that there are some "channels" along certain crystallographic directions where ions can move much more freely.

When damage to the crystal occurs the material becomes amorphous and these channels no longer exist. If these effects are not modelled or taken into account then significant error could result.

In ***ATHENA*** we simulate implantation with two different methods; an analytical look-up table approach and with a monte carlo binary collision approach (BCA). The analytical tables are well calibrated for the case of individual implants into single crystal silicon but not for cases where channeling may exist (although this effect has been implemented into the tables) or where surfaces become damaged. Alternate tables could be produced for these effects but this would rapidly become extremely difficult and knowledge of the condition of the silicon surface would have to be user controlled.

The monte carlo BCA approach, however, can simulate all these effects. The BCA module in ***ATHENA*** has been described earlier in this issue but due to its 3D based approach and its calculation of damage, multiple implants are simulated extremely accurately.

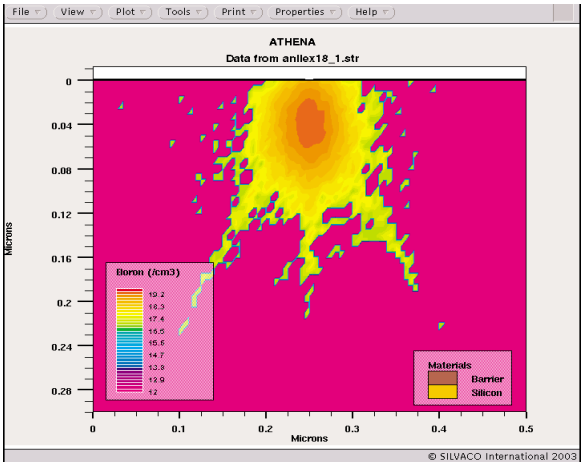

Figure 1. Simulation of two sequential implants; arsenic followed by boron. Damage to the silicon surface results in channelling in different directions and a the boron to be closer to the surface.

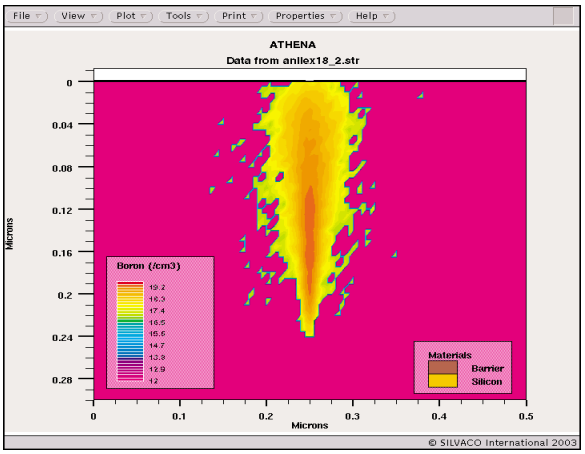

Figure 2. Simulation of two sequential implants; boron followed by arsenic. The boron is implanted into single cystal silicon wioth no damage with the result that the ions channel deeper into the silicon.

To illustrate this we can simulate the following two cases:

Case 1.

arsenic implant of 9.27e12 cm-2 ions at 10KeV
boron implant of 9.27e12 cm-2 ions at 10KeV

Case 2.

boron implant of 9.27e12 cm-2 ions at 10KeV
arsenic implant of 9.27e12 cm-2 ions at 10KeV

Figure 1 shows the results when the Athena BCA monte carlo model is used for Case 1. The arsenic implant partially disorders the silicon near the surface which means that in a boron implant immediately following the aresnic, the boron ions have a higher probability of channeling in secondary directions. The secondary directions are clearly seen in this figure.

Figure 2 shows the results when the ***ATHENA*** BCA monte carlo model is used for Case 2. The boron implant now is into well ordered single cystal silicon with only one predominant channeling direction which is normal to the surface. As a result the boron penetrates much deeper into the silion than in Case 1.

The ***ATHENA*** Monte Carlo BCA module provides users with extremely accurate profiles for single and multiple ion implants. The 3D nature of the implant is taken care of, damage effects are modelled and all this with one ***ATHENA*** command line

```
imlant arsenic dose=9.27e12 energy=10 bca
```

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