Simulation Standard

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A Journal for Circuit Simulation and SPICE Modeling Engineers

UCSD HBT SmartSpice Model Released!

SmartSpice now supports a hetrojunction bipolar transistor (HBT) model developed by the UCSD High Speed Devices Group in collaboration with a number of industrial partners [1]. The model has been available for evaluation in the form of a dynamic library for the past year. The model equations are based on a derivative of the standard SPICE Gummel-Poon model, however this model is not backward compatible with the GP model.

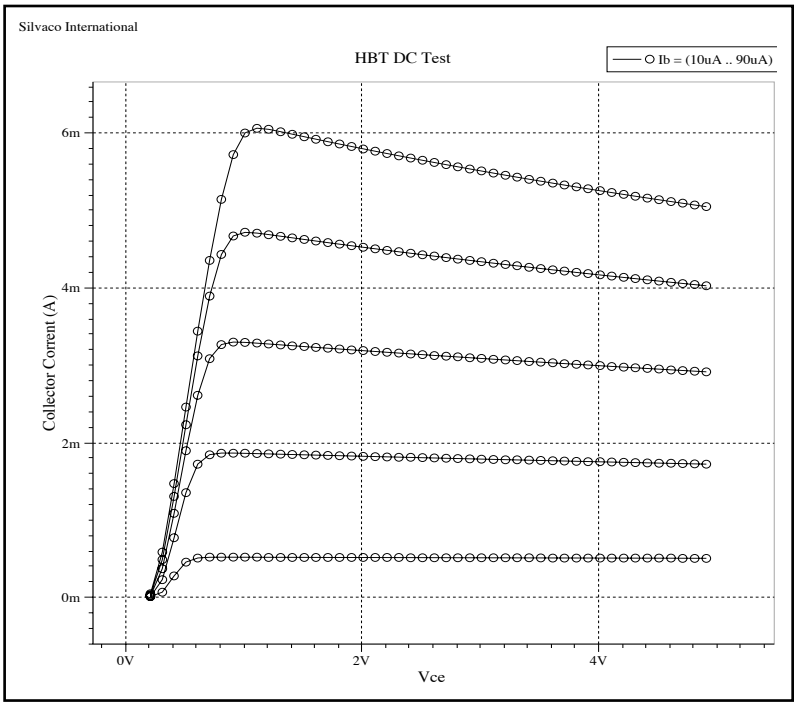

Figure 1. Ic versus Vc plot, illustrating the effect of self-heating.

The HBT model supports self-heating. The temperature of the device is a function of the power dissipated in the non-energy storage elements of the device and two model parameters (RTH and CTH). The collector current equation of the standard GP model is replaced by a more complex formulation to take into account the potential spike that can occur at the base-emitter or base-collector junction of HBTs. The HBT model supports splitting of the base and collector resistances into intrinsic and extrinsic components. Avalanche breakdown of the base-collector junction is modeled using a voltage dependent current source. Capacitances and storage times are calculated from the charge stored in the junctions as a function of collector current and junction voltages. The depletion capacitance takes into account the fact that the capacitance frequency limits at some minimum value, reached when lightly doped layers are depleted.

The HBT device is a 5 terminal device. The first four terminals are the standard collector, base, emitter and substrate of a bipolar transistor. The fifth node is an external temperature node and can be used to represent an external heat-sink or to model thermal interactions between devices. To indicate to SmartSpice that a HBT model is to be used, use "LEVEL = 20" in the .MODEL statement.

References

[1] "HBT Model Equations", http://hbt.ucsd.edu

INSIDE

Measuring Ring Oscillator Time Delay for CMOS, SOI and TFT Technologies

The Validation of AC MOS models using UTMOST was described in November 1996 issue of Simulation Standard. In this issue, the measurement technique for measuring propagation delay of a ring oscillator using UTMOST is explained.

The DC bias connection to a typical ring oscillator circuit for time period measurement is presented in Figure 1. As it can be seen, the VDD bias of the Ring oscillator is connected to HP4145 SMU for V drain and the ring oscillator ground is connected to HP4145 SMU for V source.The Output of the ring oscillator is connected to the HP54501 Digitizing Scope.

The VDD biasing for the ring oscillator is from the UTMOST "ring_osc" routine measurement setup screen (Figure 2). The ring_osc routine is located in the "Time Domain" analysis section. Press the Routine pointer arrow in the Setup and Result screen until it reads "TIME".Select the "ring_osc" routine and press the "Set Measurement" button to open the Set Measurement screen. VDD_start and VDD_step values can be defined in the setup screen and the number of steps can be specified in the Routine Control screen.

After the proper hardware connection is completed and the VDD biasing is defined in UTMOST, press the measure button in the "Extraction" screen to start the measurement. UTMOST will place the HP4145 in user mode to supply single bias point VDD to the ring oscillator circuit. After the DC biasing is established, UTMOST will control HP54501A Digital Scope to measure the T period of the oscillations. The T period values will be stored in the memory for each VDD bias point. After the last DC bias is measured, UTMOST will plot T period of the ring oscillator vs VDD bias. (Figure 3.) Following the measurement the simulation and the optimization of the ring oscillator circuit can be performed as described in the article titled "AC Model Validation Using Transient Analysis" Part 2 of Simulation Standard November 1996 issue.

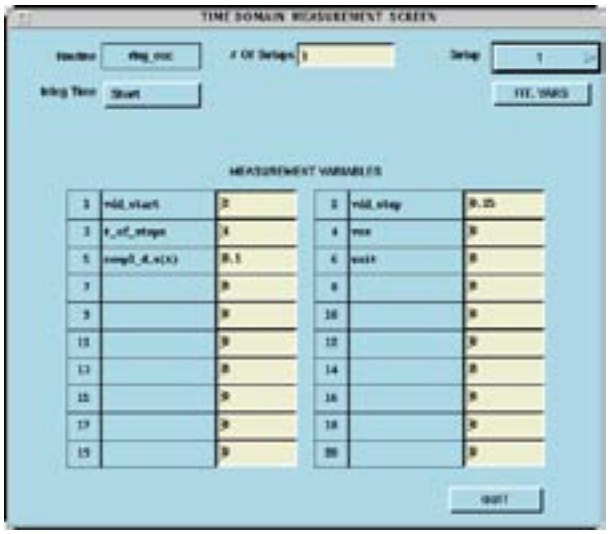

Figure 2. Ring oscillator routine measurement setup screen.

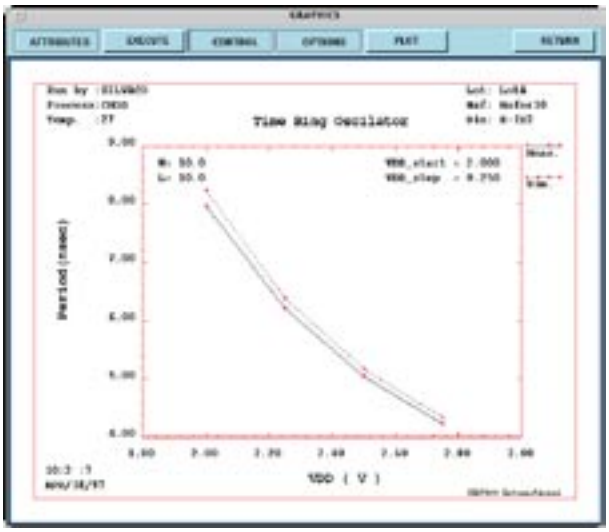

Figure 3. Measured versus simulated data of a 21 stage ring oscillator.

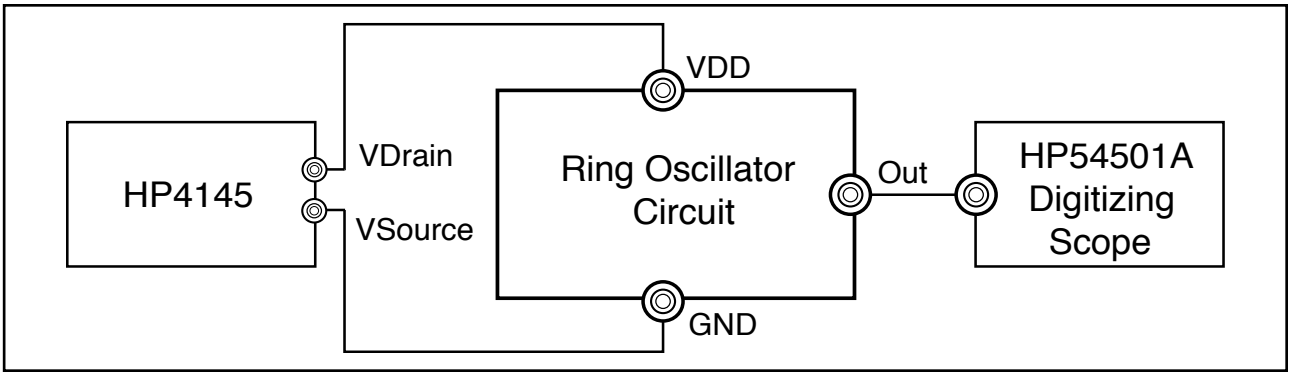

Figure 1. Typical measurement setup for measuring propagation delay of a ring oscillator on a wafer or using a packaged part.

Improved and Expanded Reedholm Interface to UTMOST

In response to numerous recent changes in the GEM and PRN file formats output by Reedholm's EMAGE program, the Reedholm interface to Utmost 12.3.5 has been substantially rewritten. One advantage of this enhancement is that the need to supply a GEM file to UTMOST has been eliminated. The PRN file format now solely supported is revision 1.06; later revisions cannot be guaranteed to be backwards compatible with the current interface.

The Reedholm interface is controlled via the Reedholm interface screen, accessed from the Utmost "Files" menu, which enables the pre-loading of a specified PRN file. All format checking is performed at this stage, and the message "Reedholm file loaded"indicates that the file has been successfully parsed. Subsequently setting the "Get Raw Data From" button on the System screen to"Reedholm File" makes the measured data available to those routines which are Reedholm-enabled.

There were twenty-one mosfet routines supported by the previous incarnation of the Reedholm interface; these routines are still supported by the new interface, and they are listed in table 1, below.Although no bipolar routines were previously supported, three of these have also now been Reedholm-enabled; these are listed in the table 2.(Note that the bipolar ALL_DC routine will only support the "All Forward" and "GP&BF" modes.)

The sequence of tests comprising a given PRN file must be consistent with the UTMOST routine to be performed; however, the order in which multiple geometries are incorporated is arbitrary. The required tests are denoted in tables 1 and 2 by their Reedholm test types, "S", "F", "E", "B" and "G", as defined in Table 3. The precise configuration of each of these tests should be inferred from the documentation for the particular routine.

UTMOST also imposes the following general requirements:

1) The EMAGE measurement mode must be set to "Fixed Scale".

2) The geometry of the device under test must be explicitly specified,in microns.

Figure 1. PRN file selection screen.

3) EMAGE uses the value "1.0000E20" to indicate a "dubious"measurement; these values will be interpreted literally by UTMOST, so it is essential that their presence be eliminated, by re-measuring or interpolating as necessary, before attempting to supply data to UTMOST.

4) The number of points measured on each curve in a multi-test routine must be invariant over the whole test sequence involved. For example,if 51 points are measured in each sweep of a given 'S' test, then 51points must also be measured in each seep of the corresponding 'F'test if the data is to be input into the MOSFET ALL_DC routine.

S = "Ids, Sweep Vds, Step Vgs & Vbs"
F = "Ids, Sweep Vgs, Step Vbs"
E = "Ids, Sweep Vgs, Step Vds"
B = "Ic, Sweep Vce, Step Ib"
G = "Gummel Plot"

Table 3: Definition of Reedholm test types.

UTMOST Routine	Reedholm Sequence	UTMOST Routine	Reedholm Sequence	UTMOST Routine	Reedholm Sequence
ID/VD-VG (1)	S	ID/VG-VB (2)	F	Leff,Rsd (3)	F
Weff (4)	F,F	VTH (5)	F	Mobility (8)	S,F
NSUB (9)	F	LAMBDA (11)	S	ETA (12)	E
VMAX (13)	E	UCRIT (14)	F	LGAMMA (16)	F
Doping (22)	F	ALL_SubV (23)	S,F,F	ALL_DC (24)	S,F
VMAXnew (25)	S	ID/VG-VD (26)	E	IDRIVE (59)	F
ISUBMAX (60)	F	BETA (79)	F	DL_new (81)	F

Table 1: Summary of supported MOSFET routines.

Utmost Routine	Reedholm Sequence	Utmost Routine	Reedholm Sequence	Utmost Routine	Reedholm Sequence
IC/VCE (1)	B	gummel (14)	G	ALL_DC (24)	B,G

Table 2: Summary of supported bipolar routines.

Simulation of SOI Analog Circuits with SmartSpice

The potential of SOI technology for high frequency and low power applications has attracted much attention. Several SPICE models for simulation of SOI MOSFETs have been developed. SmartSpice supports Honeywell SOI model(HSOI), fully depleted (FSOI) and non-fully depleted (NFSOI) SOI models by University of Florida (Gainesville), and BSIM3SOI from University of California at Berkeley. In this article we concentrate on BSIM3SOI model.

Based on the advanced BSIM3V3 extraction routine of UTMOST III, new extraction strategies have been developed to extract a complete BSIM3SOI model. The extracted model can then be optimized by using global optimization , local optimization, and multi-target rubberbanding features of UTMOST III.

Then, the final model cards can be invoked in SmartSpice to simulate any SOI analog circuit. We have succeeded in simulating a wide range of commonly used analog circuits. SmartSpice was able to provide fast and very accurate results. Several improvements have been made to the original UC-Berkeley BSIM3SOI code to solve convergence problems related to temperature modeling.

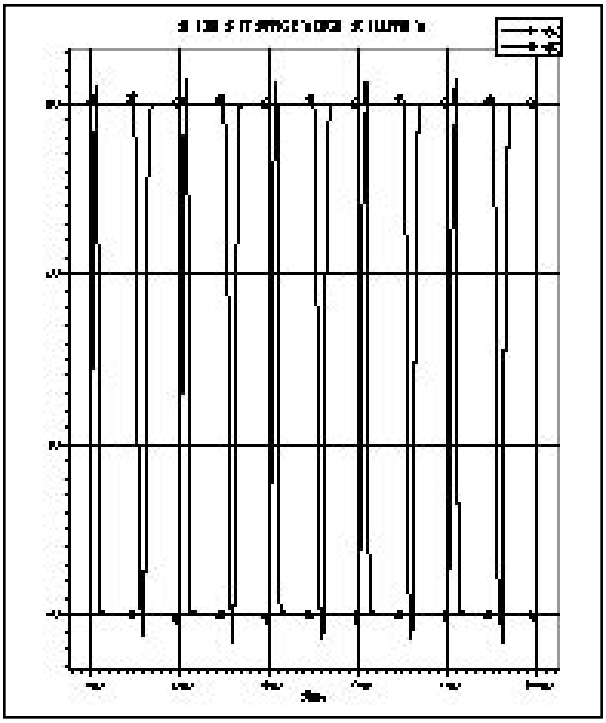

Figure 2. SmartSpice simulation result of the one-shot trigger using the BSIM3SOI model.

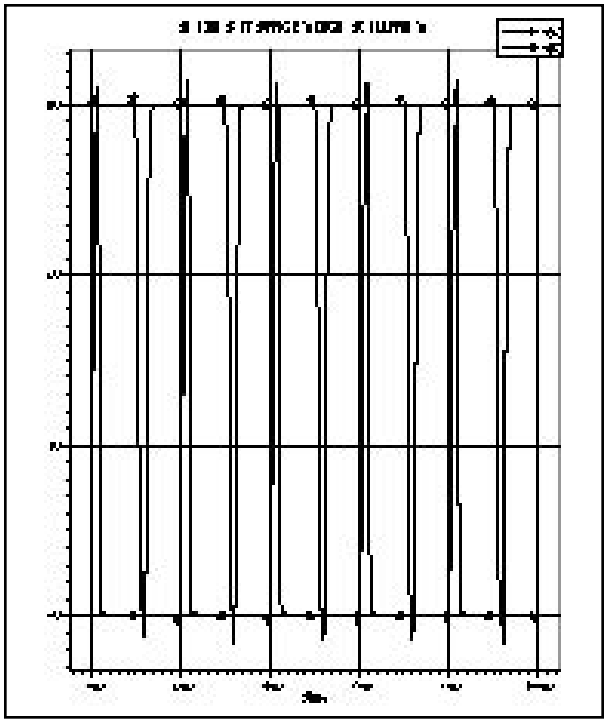

Figure 1. SmartSpice simulation result of a 17 stage ring oscillator using the BSIM3SOI model.

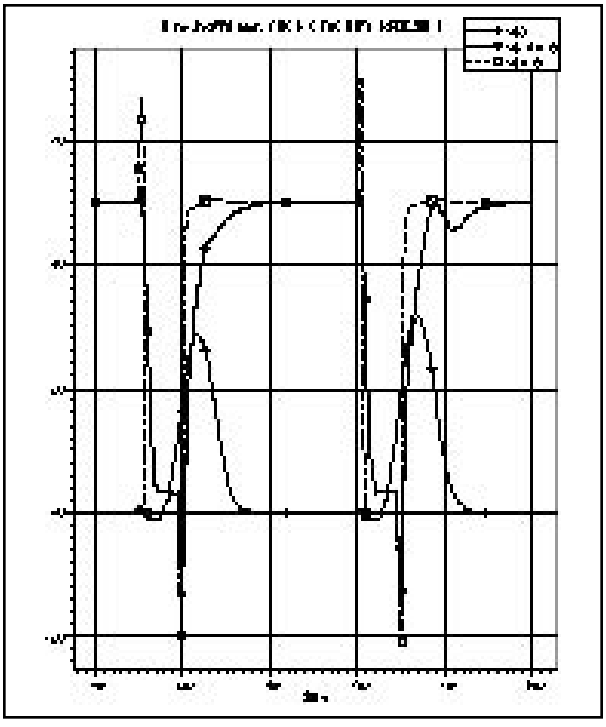

Figure 3. SmartSpice simulation result of a two-bit SOI MOSFET adder using the BSIM3 SOI model.

Simulation and Optimization of CMOS Noise Parameter

Part III

The simulation and optimization of the noise models using SPICE as a simulator is implemented in UTMOST.(Figure 1).This new feature allows UTMOST users to select *any* available SPICE noise model (including BSIM3v3 Noise models) and optimize the Noise parameters using the global optimizer.

For accurate noise simulation, UTMOST uses the SPICE interface feature through VYPER and performs ".NOISE" analysis to obtain the flicker noise versus frequency characteristics (The SPICE input deck used for Noise simulation is presented in the November 1996 issue of the Simulation Standard and it is created automatically). The simulated data is overlayed on the measured data and the rms error is displayed on the simulated versus measured curves. (Figure 2).

After adding the proper Noise selector parameter (NLEV or NOIMOD in BSIM3) the AF, KF or NOIA, NOIB and NOIC (for BSIM3 model) can be selected in the parameters screen for global optimization.

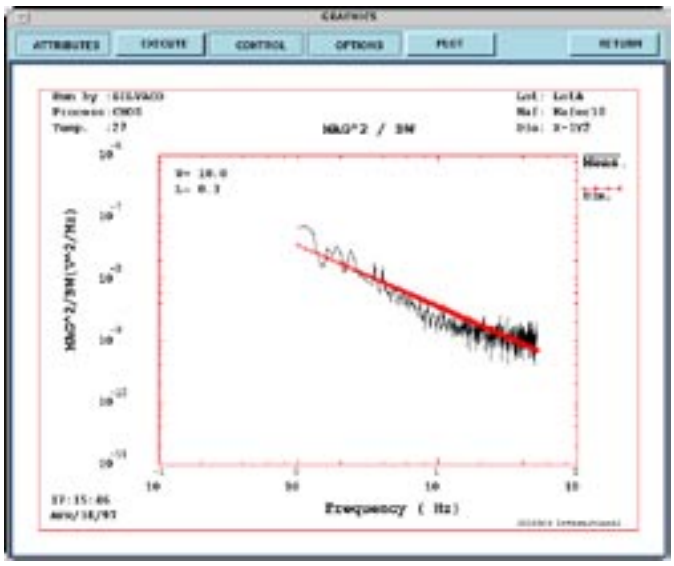

Figure 1. Measured versus simulated Flicker Noise characteristics.

Standard SPICE Flicker Noise Models:

These models are available for MOS Level1,2,3, BSIM1,BSIM2 and BSIM3v2models.

NLEV=0

$$\text{flickernoise } (v^2/Hz) = \frac{KF \cdot ids^{AF}}{COX \cdot (Leff)^2 \cdot f}$$

NLEV=1

$$\text{flickernoise } (v^2/Hz) = \frac{KF \cdot ids^{AF}}{COX \cdot Leff \cdot Weff \cdot f}$$

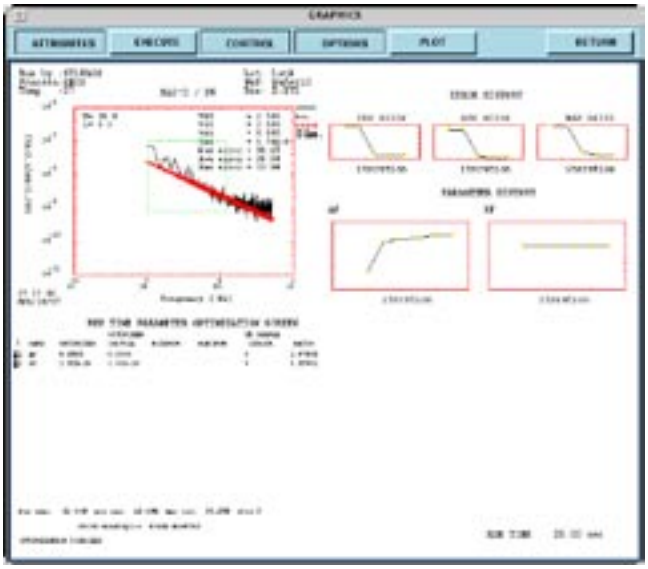

Figure 2. Global optimization selecting noise parameters AF and KF.

NLEV=2

$$\text{flickernoise } (v^2/Hz) = \frac{KF \cdot gm^2}{COX \cdot (Leff) \cdot Weff \cdot f^{AF}}$$

BSIM3V3 Flicker Noise Models:

NOIMOD=1

$$\text{flickernoise } (v^2/Hz) = \frac{KF \cdot ids^{AF}}{COX \cdot (Leff)^2 \cdot f^{EF}}$$

NOIMOD=2

$$\text{flickernoise } (v^2/Hz) = \frac{vt \cdot q^2 \cdot ids \cdot \mu eff}{f^{EF} \cdot Leff^2 \cdot COX \cdot 10^8} [Noia \cdot \log(\frac{N_0 + 2 \cdot 10^{14}}{N_l + 2 \cdot 10^{14}})$$

$$+ N_{oib} \cdot (N_0 - N_l) + 0.5 \cdot N_{oic} \cdot (N_0^2 - N_l^2)]$$

$$+ \frac{vt \cdot ids^2 \cdot \Delta L_{clm}}{f^{EF} \cdot Leff^2 \cdot Weff \cdot 10^8} \cdot \frac{N_{oia} + N_{oib} \cdot N_l + N_{oic} \cdot N_l^2}{(N_l + 2 \cdot 10^{14})^2}$$

(for complete BSIM3v3 noise equations please refer to BSIM3V3 manual.)

The DC model of the transistor should be extracted prior to the NOISE modeling/optimization because the Noise model equations will utilize the simulated DC currents and conductances based on the DC model.

Further Automation of Worst-Case SPICE Model Library Generation

The parametrized worst case model library generation is completely automated in UTMOST using "WORST CASE" button in the SPICE library generation screen.

In the traditional method of generating Typical, Slow and Fast model libraries, users vary certain process related-test parameters such as TOX, VTO, RSH and create the corner libraries. This process requires repeating the non-varying parameters for each corner model. The result is a very large library text file and since it is done manually the process is very prone to typing errors.

The parameterization of the varying model parameters eliminates the repeating. The user can have a single parametrized model file and the corner models are specified using the ".PARAM" statement. (Figure 1.)

To automatically generate a parametrized worst case model library in UTMOST, follow these steps:

- Complete the modeling of the devices and make sure that final parameters are in the "opt" column of the parameters screen.
- Select the Spice Library File option from the "Files"menu of UTMOST. This will open the Library Generation Screen.
- Press the worst case button to open "Worst Case Library Generation Screen".

Enter the Number of parameters to be parametrized. Enter the Model Parameter Name, Parametrized Name (user can specify any name) and the Typical Slow and Fast values for each parameter. For the corner parameter values a percentage or the actual value can be used.

Enter the final output worse case library file name and press the execute button to generate the file.

To add the PMOS parameters to the library, repeat the previous steps and keep the same worst case library filename before executing. The PMOS parameters will be added to the ".PARAM" statement.

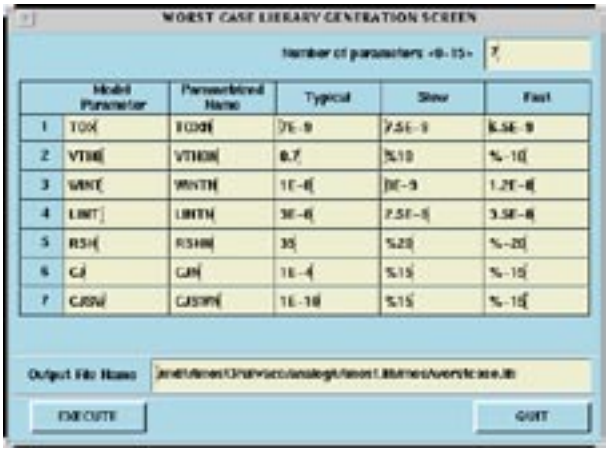

Figure 2. Worst Case Library Generation Screen.

```
.LIB CORRELATION
.PARAM
+TOXN        = 4.85e-08
+VTH0N       = 0.614541
+RSHN        = 33
+TOXP        = 4.85e-08
+VTH0P       = -0.876084
+RSHP        = 92
.ENDL CORRELATION
.LIB TT.PARAM
+TOXN        = 5e-08
+VTH0N       = 0.8
+RSHN        = 33
+TOXP        = 5e-08
+VTH0P       = -0.95
+RSHP        = 65
.ENDL TT
.LIB SS
.PARAM
+TOXN        = 5.15e-08
+VTH0N       = 0.95
+RSHN        = 50
+TOXP        = 5.15e-08
+VTH0P       = -1.1
+RSHP        = 70
.ENDL SS
.LIB FF
.PARAM
+TOXN        = 4.85e-08
+VTH0N       = 0.65
+RSHN        = 20
+TOXP        = 4.85e-08
+VTH0P       = -0.8
+RSHP        = 50
.ENDL FF
.LIB MOS
.MODEL NCH NMOS (
+LEVEL       = 8          TNOM      = 27          TOX       = TOXN
+XJ          = 3e-07      NCH       = 1.7e+17     NSUB      = 6e+16
+VTH0        = VTH0N      K1        = 1           K2        = 0
+K3          = 5.69527    K3B       = -3.02117    W0        = 1e-06
+NLX         = 1e-08      DVT0W     = 0           DVT1W     = 0
+DVT2W       = -0.032     DVT0      = 3.05586     DVT1      = 0.54
+DVT2        = -0.158023  VBM       = -10         U0        = 684.665
+UA          = 2.07679e-09 UB       = 1e-21       UC        = 3.18855e-11
+VSAT        = 80744.1    A0        = 0.602282    AGS       = 0.0618993
+B0          = 4.41845e-07 B1       = 4.41373e-06 KETA      = -0.00912594
+A1          = 0.00172021 A2        = 1.13388     RDSW      = 1504.34
+PRWG        = -0.0105225 PRWB      = 0           WR        = 1
+DWB         = 3.95557e-08 VOFF     = -0.03       NFACTOR   = 0.417307
+CIT         = 0          CDSC      = 2.4e-05     CDSCD     = 0
+CDSCB       = 0          ETA0      = 0.00135015  ETAB      = -0.099059
+DSUB        = 0.62278    PCLM      = 2.43003     PDIBLC1   = 0.113418
+PDIBLC2     = 5.77268e-05 PDIBLCB  = 0.0303625   DROUT     = 0.264402
+PSCBE1      = 1.18374e+08 PSCBE2   = 2.39058e-06 PVAG      = 0.161941
+DELTA       = 0.001      RSH       = RSHN        )
.MODEL PCH PMOS (
+LEVEL       = 49         TNOM      = 27          TOX       = TOXP
+XJ          = 3e-07      NCH       = 1.7e+17     NSUB      = 6e+16
+VTH0        = VTH0P      K1        = 0.840417    K2        = -1.28877e-05
+K3          = 15.6138    K3B       = -3.5182     W0        = 1e-06
+NLX         = 6.28758e-08 DVT0W    = 0           DVT1W     = 0
+DVT2W       = -0.032     DVT0      = 2.76674     DVT1      = 0.59632
+DVT2        = -0.131808  VBM       = -10         U0        = 265.935
+UA          = 5.30204e-09 UB       = 3e-21       UC        = -6.94601e-11
+VSAT        = 73556.2    A0        = 0.4574      AGS       = 0.0323971
+B0          = 8.07634e-07 B1       = -3.69338e-09 KETA     = -0.00855996
+A1          = 0.00172021 A2        = 1.13388     RDSW      = 8730
+PRWG        = -0.0521288 PRWB      = -0.000235835 WR       = 1
+DWB         = 1.83613e-08 VOFF     = -0.03       NFACTOR   = 0.292
+CIT         = 0          CDSC      = 0.00024     CDSCD     = 0
+CDSCB       = 0          ETA0      = 0.0483502   ETAB      = -0.0650206
+DSUB        = 0.502709   PCLM      = 4.06984     PDIBLC1   = 0.00277646
+PDIBLC2     = 1e-06      PDIBLCB   = 0.1145      DROUT     = 0.137039
+PSCBE1      = 9.55634e+08 PSCBE2   = 5e-07       PVAG      = 0.000101848
+DELTA       = 0.0181921  RSH       = RSHP        )
.ENDL MOS
```
Figure 1. Parametrized model library.

The Library generation screen creates four corner libraries in the worst case model library file: CORRELATION (extracted model parameters which were in the "opt" column of the parameters screen), TT (Typical Library), SS (Slow Library), FF (Fast Library)(Figure 1.).

New Release of PC SmartSpice

The second generation of MS-Windows based analog circuit simulator, ***SmartSpice*** Version 1.5.0 for Windows 95/NT is released. With 32-bit performance, greatly improved numerical stability, Windows interface and whole new graphical user interface (GUI) for its post-processor, ***SmartSpice*** 1.5.0 provides its users superior convergence, competitive simulation speed, high accuracy and instant productivity. This release comes with fully integrated optimizer for parametric optimization and model interpreter for user to design custom models. ***SmartSpice*** Version 1.5.0 contains fully integrated UC Berkeley BSIM3 Version 3.0 and 3.1 with significant improvements made in the BSIM3v3 Level 8.

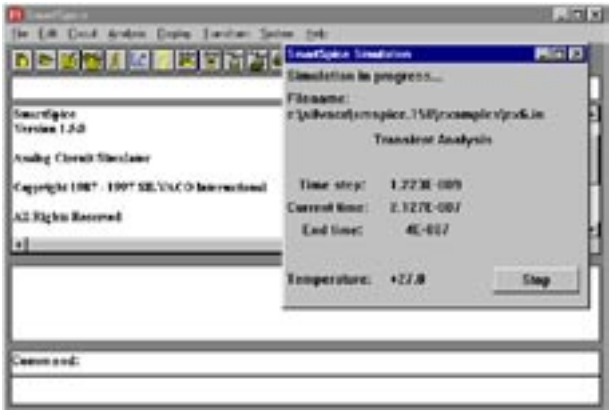

Figure 1. ***SmartSpice*** main window.

SmartSpice 1.5.0 provides all necessary analysis techniques:

- DC Analysis
- AC Small-Signal Analysis
- Transient Analysis
- Transfer Function
- Network Analysis
- Sensitivity Analysis
- Noise Analysis
- Distortion Analysis
- Fourier Analysis
- Forward and Reverse FFT
- Monte Carlo/Worst-Case Analysis
- Pole- Zero Analysis

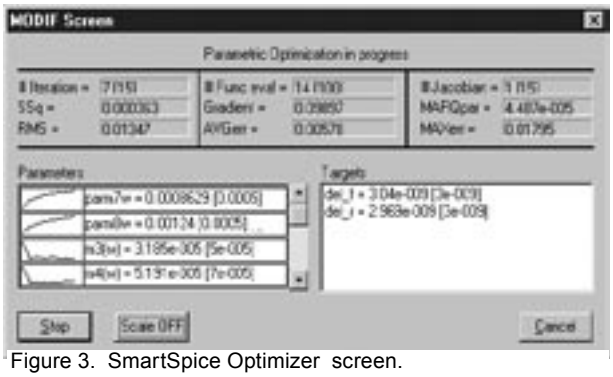

Figure 3. SmartSpice Optimizer screen.

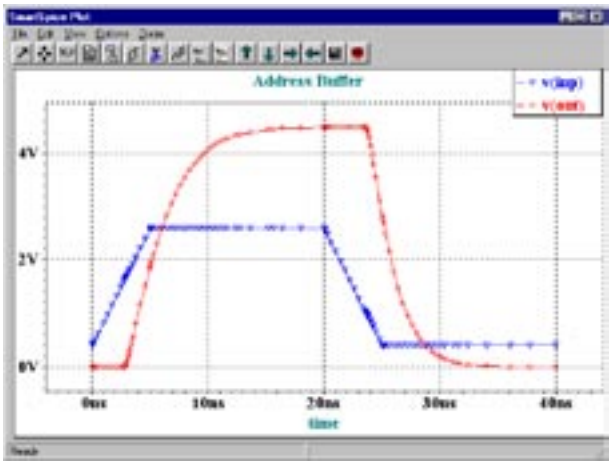

Figure 2. SmartSpice Post Processor.

Analysis dialogs, Vectors dialog, customized toolbar and on-line help have been improved in this release to allow more flexibility.

SmartSpice version 1.5.0 provides a much improved graphical post processor with new graphical user interface, enhanced measurement and display capabilities.

With a comprehensive and interactive interface for visualizing the optimization process, the fully integrated optimizer provides user with run-time graphical feedback and greatly helps users with their high-performance circuit design. The optimizer can fine-tune delay, rise/fall times, trip points, max/min current, and any other circuit performance measure.

SmartSpice is also tightly integrated into Viewlogic® Workview Office to offer better simulation solutions. OLE technology is used to bring seamless integration between SmartSpice and schematic front-end. Additional integration effort for other Schematic Capture tools are underway. Engineers will be able to benefit from advanced simulation technology. SmartSpice offers within their familiar design environment.

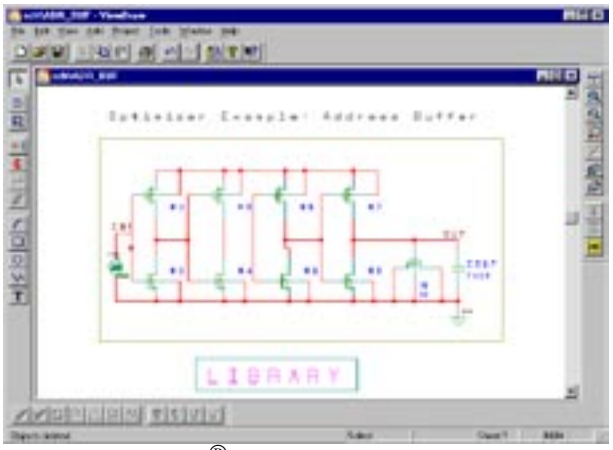

Figure 4. Viewlogic® schematic entry.

Diagnose Process Variations By Using SPC Charts and a Wafer Map

Introduction

Timely delivery of high quality products at a low cost to the market is the key to the success of VLSI business. Quality control charts have been proven to be very useful in monitoring the quality of the products and assisting in finding the possible causes of process deviations from normal values. In this article we demonstrate how to use the combination of statistical process control charts (SPC) and a wafer map display in order to assist process and integration engineers identify possible process steps that cause low yield.

SPC Chart to Identify Out of Control Points

In this article we are going to utilize a data set that consists of leakage measurement data to demonstrate how to identify out-of-control datapoints. After loading a dataset into SPAYN, an attribute search is performed to get the 999 sets of data collected from Lot1. Nine wafers from this particular lot were measured. From the Charts menu, invoke the SPC chart. The statistical data of the controlled measurement is used to define the control limits. All available data should be used to determine the control limits. If the process is in statistical control, the control chart will show random oscillations without any definable pattern. A point outside the control limits, or some visible trend such as a sequence of points on one side of the center line signals that the process is going out of control. In Figure 1, we see that the average value from Wafer six is outside the limits. The control charts only signal a problem, they do not in any way reveal the cause. To find the cause of process problems, we need to use the wafer map display of the parameter in order to obtain more information.

Spatial Distribution On A Wafer

Perform Data Search->Search Results->Wafer Map... operations to invoke the wafer map. If the data file was originally generated using UTMOST, then the die location information is already available in the die name. Load the die location as UTMOST which means no additional die location file is needed. SPAYN will read the die location information from the die name. By using the SetUp feature on the wafer map window select the particular wafer for analysis. Lets select wafer six. Then display the Id_leak values on the wafer map (Figure 3). This display gives the spatial distribution of Id_leak values on a wafer map. By using different colors to represent different ranges of values, an indication of the cause of low yield is obtained. In this display of Id_leak, one could easily see that high values of leakage current are distributed towards the boundary, especially the right side of ring of the wafer which is a strong indication that there are some problems with some of the process steps. So we could draw the conclusion that something must be modified on the etching, thermal cycle, or implanter setup which could possibly contributed to such a pattern.

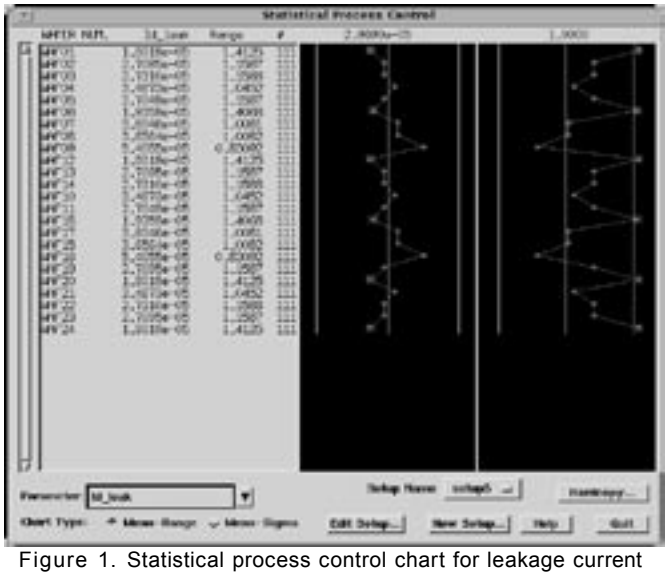

Figure 1. Statistical process control chart for leakage current as a function of wafer number.

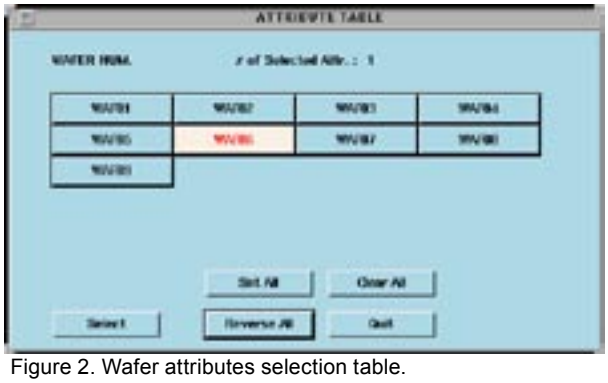

Figure 2. Wafer attributes selection table.

Figure 3. Wafer Map display showing distribution of leakage current.

Diagnose Process Variations By Using Wafer Map and Highlighted Histogram Plot

Introduction

Cross wafer parametric variation can be a significant source of yield loss in IC manufcturing. Often cross-wafer problems are not seen as the data is lost when 'wafer averages' are taken in simple statistical analyses. This new wafer map feature in SPAYN is a useful tool that can assist process and integration engineers to find out process steps that cause the cross wafer yield loss.

Lot Distribution

As an example a SPICE Level 3 data set for a CMOS process is used. After loading the data into SPAYN, an attribute search is performed in order to get 107 sets of data collected from Lot1. Five wafers were sampled in this case. After a parameter search, invoke the histogram plot feature to display the parameters. LD for NMOS was selected as an example. The histogram plot displays the lot distribution of LD_N. A more useful plot would be a display of how the LD_N values are distributed access different wafers. By using the Highlighted by Attribute feature from the Set Up menu bar, we could generate a highlighted histogram plot by plotting the values of LD_N from different wafers by different colors. As indicated in Figure 3, the lightest grey color is used for wafer two. Notice that the values sampled from wafer two are distributed to the lower part of the distribution. Some are close to the nominal value, some are quite low. At this point, we want to know what are the process steps that cause such a low value. This is where the wafer map feature can be used.

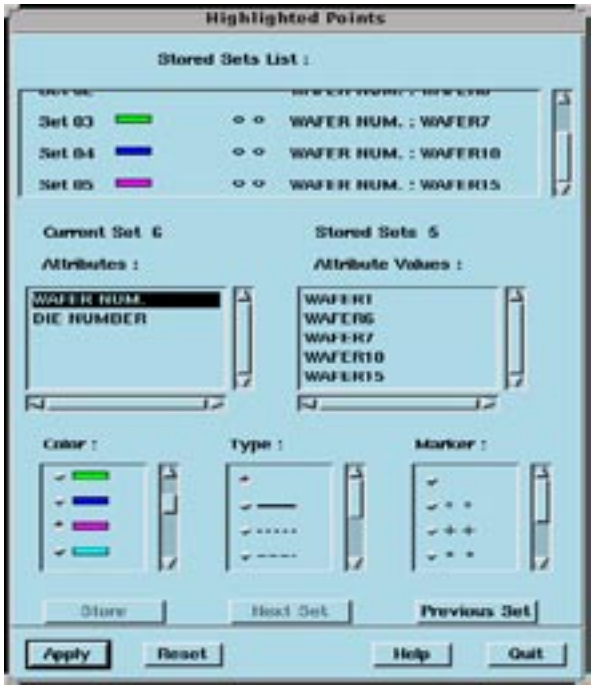

Figure 2. Setup window for highlighting histogram window by selecting attributes.

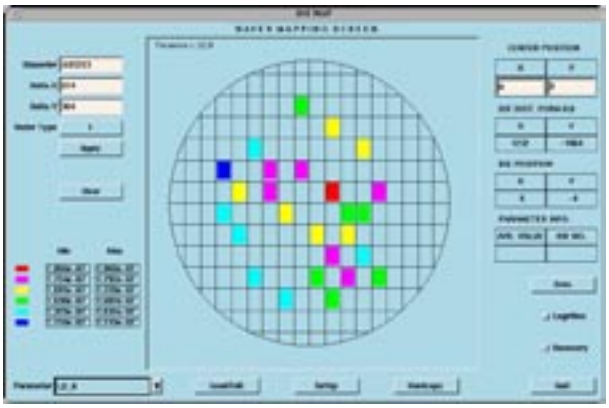

Figure 1. Wafer Map display of statistically correlated parameter values for LD_N parameter.

Spatial Distribution On A Wafer

Perform Data Search -> Search Results-> Wafer Map... operations to invoke the wafer map. The die location information that was saved in a separate file is now loaded into SPAYN in the wafer map window. By using the SetUp feature on the wafer map window, one can select a particular wafer for analysis. For this analysis, wafer 2 was selected. Then display the LD_N values on the wafer map. This display gives the spatial distribution of LD_N values on a wafer map. By selecting different colors to represent different ranges of values, user can get an indication for the cause of low values. In our display of LD_N, we could easily see lower values are distributed toward the left side of the wafer which is a strong indication that there are some problems with some of the process steps. A yield or process engineer can use this data to identify which process steps have connections to this data skew.

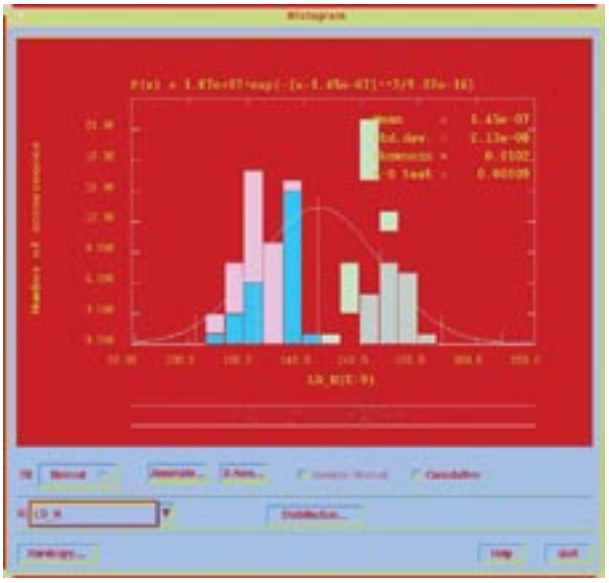

Figure 3. Highlighted histogram display of parameter values.

Calendar of Events

March

1	
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5	Workshop - Santa Clara
6	Workshop - Phoenix
7	Workshop - Austin
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12	Workshop - Santa Clara
13	Workshop - Phoenix Workshop - Guildford
14	Workshop - Austin
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19	Workshop - Santa Clara
20	Workshop - Phoenix
21	Workshop - Austin
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26	Workshop - Santa Clara
27	Workshop - Phoenix Workshop - Grenoble
28	Workshop - Austin
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April

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4	Workshop - Japan
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10	Workshop - Munich
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17	UTMOST Workshop - Japan
18	P/D Workshop - Japan
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24	Workshop - Grenoble
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Bulletin Board

Poster Presentation at IWSM!

Mr. Itaru Kamohara, Silvao Japan application engineer will present a poster titled *"Statistical Simulation Methodology for Multi-Level Interconnect Contact Analysis and Step Coverage Evaluation"* at the second IWSM, to be held at Kyoto, Japan, on June 6 to 8.

Paper Presentation at ULSI Technology Systems!

Mr. Chau-Neng Wu, Silvaco Taiwan application engineer will present a paper titled *" Efficient Output ESD Protection of High-Speed SRAM IC with Well-Coupled Technique in Sub-μm CMOS Technology"* at the VLSI Technology Systems and Applications Symposium to be held at Taipei, Taiwan on June 3 to 5.

Silvaco Japan Moves and Expands!

Rapid growth of Silvaco Japan necessitated a move of the offices to much larger quarters. The new office will accommodate a large training room for weekly workshops (for 30 engineers), 50 employees and a large computer center to serve as a computational hub for Silvaco Far East operations. The new address and phone numbers are:

Silvaco Japan
Miyake Building 4F
549-2 Shinano-cho
Totsuka, Yokohama 244
Japan
Phone: (45) 820-3000
Fax (45) 820-3005

Visit Silvaco at CICC for SmartSpice Demo!

CICC conference will be held May 5 to 8 at the Santa Clara Conventions Center located in booth #12. Silvaco will exhibit its premiere products for Analog Circuit Design. Special focus will be on SmartSpice analog circuit simulation.

For more information on any of our workshops, please check our web site at ***http://www.silvaco.com***

Hints, Tips and Solutions

Mustafa Taner, Applications and Support Engineer

Q. How can I make BSIM3 extraction routine to provide defined VGS steps for IDS vs VDS characteristics?

A. The BSIM3 extraction routine in UTMOST performs four different types of measurements for each selected geometry. There are two IDS vs VGS (low and high VDS) and two IDS vs VDS (0V and high VBS) measurements. The first measurement of the BSIM3 parameter extraction routine is the IDS vs VGS measurement at low VDS. The BISM3 routine will extract the VT from the IDS vs VGS measurements and VT + VG_strt_offset will define the first VGS step for the following IDS vs VDS characteristics. The user can also specify the maximum VGS bias using the VGS_stop variable. However the intermediate VG steps will be calculated based on the VGS_start and VGS_stop values. The threshold voltage (VT) will vary for different geometries and as a result each device will have different VGS_steps. In addition, the VGS_steps may sometimes have 3 digits after the decimal point depending on the extracted VT and the maximum VGS. This methodology is essential for the BSIM3 routine to extract proper model parameters. However, if the user would like to define the VGS_start bias rather than allowing UTMOST to calculate it or maintain uniform VGS steps for every geometry, then the Fit Variables can be utilized to provide this option.

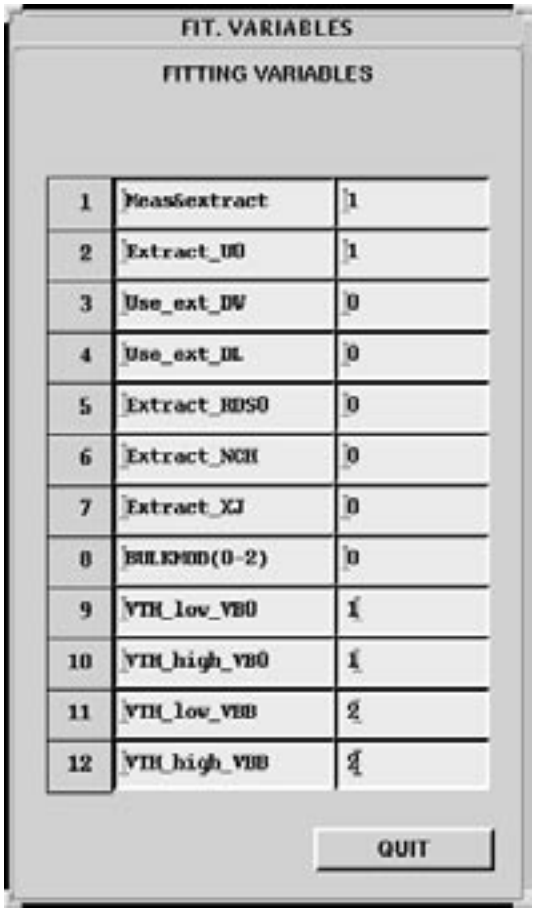

Figure 1. BSIM3 Fit Variables Screen.

To open the Fit variables screen for BSIM3 routine press the "setups" button from the main UTMOST screen and select the BSIM3 routine. Press the "Set Measurement" button to open the set measurement screen for the BSIM3 routine. The Firt Variable button is located on the top right corner of the BSIM3 set measurement screen. The last four Fitting variables in the Fit variables screen are used to define boundaries for the VT extraction. This feature was implemented to prevent accidental destruction of devices when the VT was incorrectly extracted due to the bad IDS vs VGS data.The variables VTH_low_VB0, VTH_highVB0, VTH_low_VBB and VTH_high_VBB can also be utilized to force a specific VGS_start value (Figure 1).

For example: If the user would like to define VGS_start to be 1V for the IDS vs VDS characteristics at VBS=0V and 2V at VBS=high,then the variables VTH_low_VB0 and VTH_highVB0 should be equal to 1 and the variables VTH_low_VBB and VTH_high_VBB should be equal to 2.The VGS_strt_off variable in the Measurement setup screen should be set to 0. In this setup, (assuming that VGS maximum is equal to 5V and and the #_of VG steps is 5) the VGS steps will be 1V and 0.75V even for the IDS vs VDS characteristics at VBS=0 and VBS=high respectively.

Call for Questions

If you have hints, tips, solutions or questions to contribute, please contact our Applications and Support Department

Phone: (408) 567-1000 Fax: (408) 496-6080

e-mail: *support@silvaco.com*

Hints, Tips and Solutions Archive

Check our our Web Page to see more details of this example plus an archive of previous Hints, Tips, and Solutions

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