Full PDK development services providing foundry-specific models, symbols, rule decks, and parameterized cells (P-cells).

**EDA Tools in Custom IC Design Services**

- Gateway Schematic Editor
- SmartSpice Circuit Simulator
- Expert Layout Editor
- Guardian DRC/LVS/LPE
- HIPEX Full-chip Parasitic Extraction
- LISA Scripting Language

**PDK Development Service Deliverables**

**Schematic Symbols** — for the Gateway Schematic Editor to invoke Parameterized Cells in the Expert Layout design tool that are DRC and LVS correct. These parameterized symbols and respective subcircuits are integrated and tested with the SPICE models to assure a standard convention for transistor level simulation. PCells are written in the LISA Scripting Language.

**SPICE Models** — SPICE model (optional) files, verified with the SmartSpice Circuit Simulator, at the foundry-supplied process corners (temperature, voltage, process). Silvaco will extract one set of models from a wafer or measured data and produce a complete measured vs. simulation report for each device.

**Technology Files** — layer files that correlate the legal GDSII layers for each of the process layers for layout and verification tools. Display files to customize the layout and schematic tools for GDS layers, display colors and user-customizable hot keys.

**Rule Decks** — contain the layout rules encoded into the format used by the Expert Layout Editor, Guardian DRC/LVS/LPE tools, and the HIPEX Full-chip Parasitic Extractor.

**Parameterized Cells** — enable annotated device schematics to be automatically drawn in the Expert Layout Editor, DRC and LVS correct, using the LISA scripting language.
Foundry Design Data for PDK Development

Services

- Foundry supplied wafer with test chip document (or measured results for all corners) process related parameter variation, and test circuit netlist for model validation
- Specifications, layout examples, scripts, and parameterized cell descriptions for targeted devices including resistors, capacitors, diodes, NMOS and PMOS transistors, NPN and PNP bipolar transistors, inductors, and varactors
- DRC, LVS, LPE rule documents and DRC, LVS, LPE decks (e.g. Dracula™) technology files, display files, and any scripts or utilities to prepare foundry data for customer use
- Process and design documents for electrical parameters, noise, matching, test and reliability data
- Process specification for layers, including process options

Silvaco PDK-driven EDA Tool Flow from Schematic to Layout to Final Simulation

A. Bandgap circuit captured with Gateway Schematic Editor using symbols from the PDK.

B. Pcells are instantiated by Expert Layout Editor with flight lines and placed to final layout.

C. SmartSpice simulates extracted bandgap over temperature.