

MOS Device SPICE Modeling Service Questionnaire

Please fill out the following questionnaire. The data you provide in this form is necessary for Silvaco to supply you with high quality SPICE models.

Contact Person in Your Company

(for technical questions)

NAME: _____

COMPANY: _____

PHONE: _____

FAX: _____

EMAIL: _____

Package Part or Wafer Information:

For packaged parts please specify package type:

For wafer, please specify:

How many wafers will be supplied?: _____

Wafer #: _____

Lot#: _____

Are the devices in a scribeline or in a drop-in test die?:

Model Type

Please specify the SPICE model type (For example: HiSIM, PSP, BSIM3, BSIM4, etc.)

Please specify the circuit simulator(including the version number) for which the models are generated.

Bias Conditions

Please specify the maximum bias conditions to apply for MODELING purposes. (Make sure the specified bias conditions are not destructive for the shortest channel length device over the temperature.

	NMOS	PMOS
Max VDS:	_____	_____
Max VGS:	_____	_____
Max VBS:	_____	_____

Please include measured data plots of IDS/VDSmax @ VBS=0V, IDS/VDSmax @ VBSmax and IDS/VGS @ VBS steps from 0V to VBSmax.

Temperature Conditions

Please specify the temperature points for devices to be characterized?

(For example: 0 C, 27 C, 85 C):

Process and Layout Related Information

Please provide the following information for the supplied wafer or the packaged parts.

	NTYPE	PTYPE
TOX:	_____	_____
VT0:	_____	_____
NCH: (surface concentration)	_____	_____
NSUB: (bulk (below surface) concentration)	_____	_____
XJ: (junction depth)	_____	_____
HDIF: (middle of contact to gate (poly) distance)	_____	_____
RSH:	_____	_____

Test Chip Information

Please list the MOS devices in the test chip. (If there are more than 10 devices please specify only 10 critical devices.):

	NTYPE (μm)		PTYPE (μm)	
	W	L	W	L
1)	_____	_____	_____	_____
2)	_____	_____	_____	_____
3)	_____	_____	_____	_____
4)	_____	_____	_____	_____
5)	_____	_____	_____	_____
6)	_____	_____	_____	_____
7)	_____	_____	_____	_____
8)	_____	_____	_____	_____
9)	_____	_____	_____	_____
10)	_____	_____	_____	_____

Are there area and periphery diode structures to measure Area (CJ) and Sidewall (CJSW) capacitance? (If yes, please indicate the location of these structures on the test chip.)

Are there structures to measure overlap capacitances? (If yes, please indicate the location of these structures on the test chip.)

Is there a Ring Oscillator circuit available for AC model validation? (If yes, please indicate the location of these structures on the test chip.)

Worst Case Corner Information

Please provide the following information for the worst case corner model generation: If the exact numbers are not available please enter the variation in percentage. If data is not available enter: N/A.

	NTYPE			PTYPE		
	min.	typ.	max	min.	typ.	max
TOX	_____	_____	_____	_____	_____	_____
VT0	_____	_____	_____	_____	_____	_____
DL (total diffusion)	_____	_____	_____	_____	_____	_____
DW (total diffusion)	_____	_____	_____	_____	_____	_____
RSH (N+ for NTYPE) (P+ for PTYPE)	_____	_____	_____	_____	_____	_____
IDSAT (specify IDSAT measured bias conditions and device geometry)	_____	_____	_____	_____	_____	_____
Bias Conditions	_____	_____	_____	_____	_____	_____
W/L	_____	_____	_____	_____	_____	_____
CJ	_____	_____	_____	_____	_____	_____
CJSW	_____	_____	_____	_____	_____	_____
CGDO	_____	_____	_____	_____	_____	_____
CGSO	_____	_____	_____	_____	_____	_____

Please add more parameters' variation (such as NCH (surface conc.), NSUB (bulk conc.), UO (mobility), etc.) if available.

If you have any questions please contact:

SPICE Modeling Group
email: spicemodeling@silvaco.com

SILVACO

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