

SILVACO

FULL-CHIP PARASITIC EXTRACTION

HIPEX

HIPEX is an accurate and fast full-chip hierarchical extraction software that performs extraction of parasitic capacitances and resistances from hierarchical layouts. HIPEX is tightly integrated with the Expert Layout Editor for complete design flow of DRC/LVS and RC parasitic extraction.

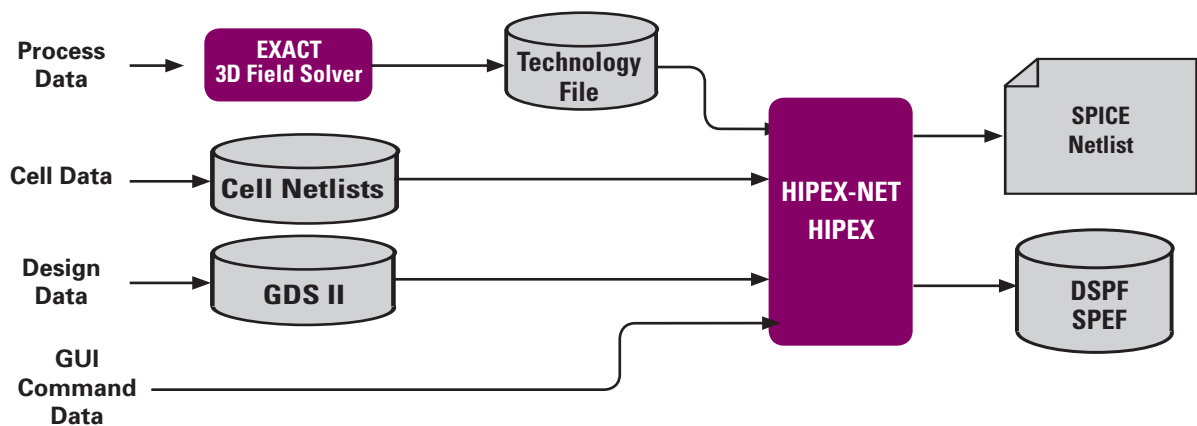


- **Multiple parasitic extraction models, including lumped RC, C only, R only, coupled C and fully distributed RC**
- **Selected net extraction for fast RC extraction of critical path nets in SoCs and large memories**
- **Efficient network reduction for distributed parasitic RC networks**
- **Output parasitic netlist files in SPICE, back-annotated netlist, DSPF and SPEF formats**
- **Automated back annotation enables accurate post-layout simulation and analysis**
- **Parasitic device extraction on both transistor and gate levels**

HIPEX-NET Device Extraction

- Integrated into Expert Layout Editor
- Converters for Dracula technology files
- Common Graphical User Interface for Solaris, Linux and Windows platforms
- Extracts hierarchical netlist preserving original layout hierarchy for easy analysis
- Extracts MOSFET, MESFET, BJT, JFET, diode, capacitor, resistor, and parameterized user-defined devices
- Performs electrical rule checking (ERC) for shorts, opens, dangles
- Accurate device extraction for non-45 and non-90 degrees devices
- Efficient memory usage for handling large designs
- Available in 32 and 64 bit versions
- HIPEX-NET is not multi-threaded

HIPEX Full-Chip Parasitic Extractor Product Design Flow

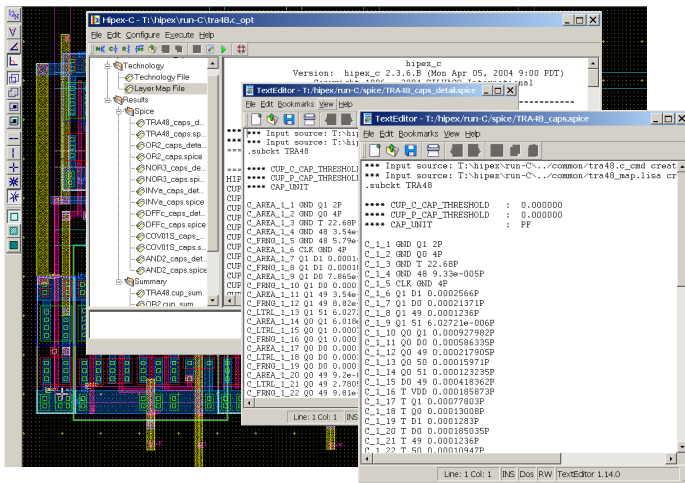


HIPEX Parasitic Capacitance Extraction

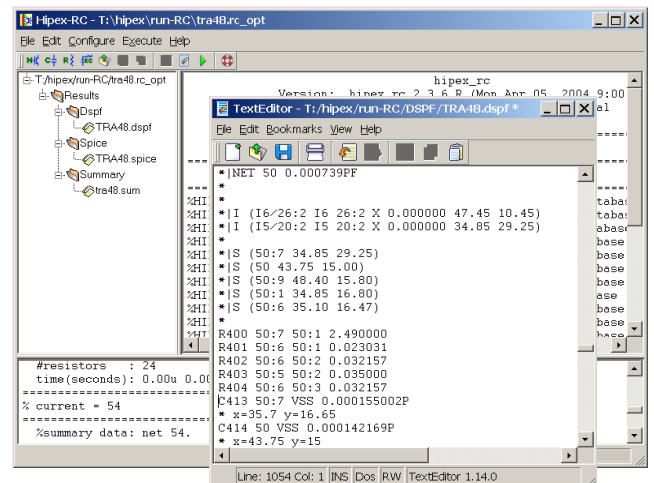
- Driven by rule-based technology file
- Back-annotates the schematic netlist with parasitic capacitors
- Striping algorithm and stripe database enables efficient parallelization for multi-processor machines
- Extracts parasitic coupling capacitors for full chip and selected nets
- Offers user-defined or built-in capacitance models to trade off between accuracy and run time
- Supports external capacitance rule files generated by EXACT for 3D accurate mode
- Creates incremental capacitance database on a net-by-net basis
- Extracts selected nets for fast parasitic C computation of critical paths

HIPEX Parasitic Resistance Extraction

- Driven by rule-based technology file
- Back-annotates the schematic netlist with parasitic resistors
- Extracts contact parasitic resistors
- Processes L, T, Cross and Bend resistor shapes
- Uses contact over-sizing and clustering to simplify resistor shapes.
- Extracts netlist with parasitic resistors hierarchically for full chip or selected nodes
- Creates incremental resistance database on a net-by-net basis
- Multiple extraction models and equation solvers are used for arbitrary shape resistors
- Splits long conducting tracks for more accurate RC distribution
- Provides output of selected nodes into GDS or CIF file for layout debugging purposes



HIPEX-C provides detailed coupling capacitor netlists for accurate analyses of overlap, lateral, and fringe capacitances.



HIPEX supports SPICE, DSPF, or SPEF formats.

HIPEX Parasitic Network Distribution

- Combines extracted resistance with newly created nodes and parasitic capacitance
- User-defined threshold for minimum resistance and capacitance
- Distributes capacitors over parasitic resistor bodies accurately using XY coordinates
- Uses PI model for RC network
- Results are output to SPICE, DSPF and SPEF netlists
- Back-annotates schematic netlist with parasitic resistors and capacitors
- Outputs distributed parasitic capacitors in coupling mode

HIPEX-CRC Network Reduction Tool

- Significantly reduces runtime of post-layout and post-route simulations
- Performs reduction by elimination of dangling RC elements, elimination of RC elements less than a user specified threshold, parallel/series merging and Scattering-Parameter-Based Macromodeling
- Performs networks reduction in linear time
- Handles RC networks with loops
- Preserves the same accuracy of simulation for reduced RC networks
- Supports SPICE, DSPF, or SPEF formats
- Custom reduction algorithms using LISA Scripting Language for selecting subcircuits, cells, nets and thresholds

HIPEX Inputs/Outputs



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