Catalyst AD

SPICE Netlist to Verilog Gates Converter

The premier tool for converting transistor-level designs into verilog gate-level representations with applications in microprocessor, DSP, graphics and high-speed communication markets.

- **Provides an automated solution for generating gate-level verilog netlists and models from transistor netlists**
- **Ideal for reverse-engineering legacy hard IP and custom logic for design reuse and migration**
- **Supports HSPICE™/SPECTRE™ and DSPF hierarchical or flat netlists**
- **Handles all classes of CMOS/SOI design styles (standard cell, custom, static, dynamic, combinational, sequential, domino, footed, footless, self-timed, post-charged, cascode, DCVS, pass transistor, barrel-shifters, cross-bar switching structures, m-of-n logic trees, etc.)**
- **Controls proper modeling of wide fan-in pass-gates of 24 inputs or more, sneak paths and output path depths containing hundreds of thousands of parallel paths**
- **Catalyst AD and AccuCore together deliver a complete verification and timing modeling solution**

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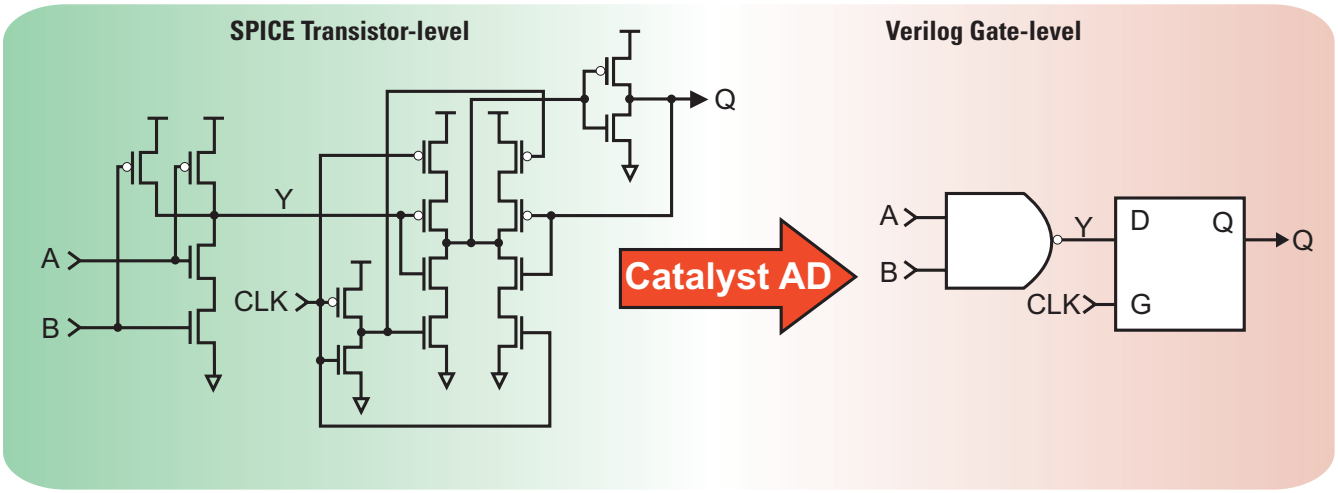
Features

- Easily handles multi-million-transistor netlists
- Automatic function extraction of full custom and hard IP blocks
- Generates gate-level simulation and synthesis verilog netlist and models
- Supports HSPICE™/SPECTRE™ and DSPF hierarchical or flat netlists
- Easy to use batch mode Tcl script and config file interface



Automatic gate-level funtion extraction from a transistor-level netlist.

Tool Flow Steps

1. Read a SPICE/DSPF netlist flattening if necessary, preserving module, port and net names and busses with full hierarchical path info.
2. Derive clocks from non-static elements such as clock dividers, clock doublers, phase shifters and PLLs, perform clock propagation via Boolean analysis, and identify the subsequent nodes that are clock nodes honoring stop clock propagation through a particular node.
3. Isolating analog circuits from logic via black-box naming user-defined patterns.
4. Automatically recognize the latch and flip-flop structures and variations.
5. Partition the design into cells.
6. Performs automatic algorithmic and pattern based function extraction and cell classification.
7. Generate structural verilog cell netlist with optional “black-boxed” components.
8. Generate gate-level verilog models.

Inputs

- A hierarchical or flat SPICE/DSPF netlist, with optional RC information
- A .cfg configuration file with command & variable settings, pin info and file names
- A basic .tcl run-time script file

Outputs

- Structural verilog cell netlist
- Gate-level verilog model library
- Verilog template library

Input files:

Example and.cfg input file:

```
inputs a b c
outputs out
powers vdd
grounds gnd
TOP_VLOG_MODULE and
TOP_SPICE_SUBCKT and
IN_FILE_NAME and.cir
MOSFET_TYPE p pmos
MOSFET_TYPE n nmos
```

Example and.tcl input file:

```
gen_model and.cfg
```

Run-time command:

```
catalystad and.tcl |& tee and.log
```

Output files:

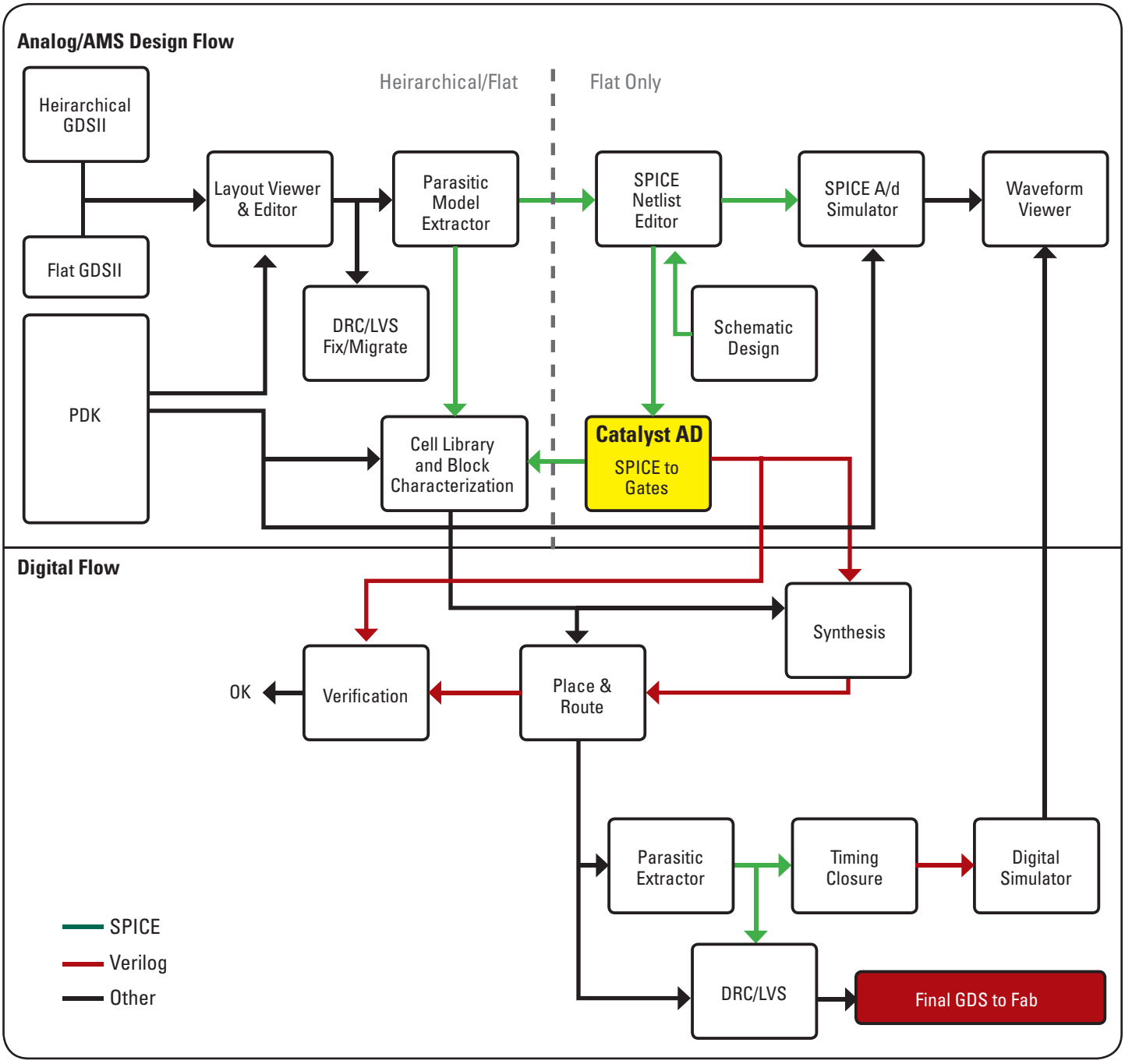
Example and.v netlist output file:

```
module and( out , a , b , c );
output out ;
input a , b , c ;
supply1 vdd ;
supply0 gnd ;
wire z;
and_dc_2 i_and_dc_2( .z(z) , .a(a) , .b(b) , .c(c) );
and_dc_3 i_and_dc_3( .out(out) , .z(z) );
endmodule
```

Example and_vlg.lib model output file (partial):

```
`include “template.v”
`celldefine
module and_dc_2( z , \a<1> , \a<0> );
output z ;
input \a<1> , \a<0> ;
// gate type static for z
wire net_z_1_0 ;
wire z_out_0 ;
wire net_z_1_1 ;
wire z_out_1 ;
buf ( net_z_1_0 , \a<0> );
mux mux_inst_z_0_0 ( z_out_0 , \a<1> , 1’b0 , net_z_1_0 );
not ( net_z_1_1 , \a<0> );
mux mux_inst_z_0_1 ( z_out_1 , \a<1> , 1’b1 , net_z_1_1 );
// inverter for 0 term
wire z_out_0_bar ;
not ( z_out_0_bar , z_out_0 );
// output driver
and ( z , z_out_0_bar , z_out_1 );
endmodule
`endcelldefine
```

Design Center Tool Flow



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