AccuCell is an accurate, automated, fast and flexible software tool for characterizing and validating standard cell, I/O, and custom cell libraries.

- Generates accurate single-pass, state-dependent timing, power, leakage and noise Liberty™ .lib libraries for advanced VDSM technologies
- Supports the latest designs in both static and dynamic cells
- State-of-the-art automatic function recognition and vector generation for easy setup of config files
- Characterization can be run in parallel on either multi-core machines or over a network by using Sun Grid Engine (SGE)
- Includes fast API-based SmartSpice characterization engine
**Automation and Ease of Use**

- Powerful scripting environment permits specification of all cell and simulator characterization and library creation options
- Powerful multi-corner characterization mode for single-pass characterization of all conditions
- Netlist screening option for valid input circuits traps and avoids timely errors
- Support the latest in both static and dynamic styles (multi-voltage, multi-clock, clock enable, gated clock, multi-data, scan enable, one-hot mux, multi-output) cells
- Automated setup from an existing .lib template for easy library re-characterization
- Automatic state-based input pin capacitance measurement with multiple reporting options
- Automated maximum capacitance and slope determination with or without variable slew or delay degradation

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**AccuCell Cell Characterization and Modeling**

**Cell Design**

- Schematic and/or Layout

**Extracted Netlist**

**Characterization and Modeling**

- Function Extraction
- Vector, Slope, Load Generation
- Characterization
- Modeling
- Library Validation

**Cell Based Design**

- Logic Synthesis
- Gate Level Simulation
- Floorplanning
- Place and Route
- Static Timing Analysis
- Signal Integrity
- ATPG

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**Advanced Capabilities**

- Advanced SOI and un-buffered input options
- Supports advanced multi-point slope or active-driver input stimulus for accurate VDSM characterization
- “ASIC” flow for simplified unified cell library characterization conditions
- Support for active loads for accurate low voltage measurement and user defined passive and active non-linear loading effects
- Advanced fast evaluation of setup & hold, recovery & removal and minimum pulse width characteristics with extension characterization options supports both static and dynamic storage circuits with level, edge and pulsed inputs with multiple clocks
- Tri-state driver characterization supports both conductance or current measurement
- State-of-the-art strength and state-based Ordered Binary Decision Diagram (OBDD) method automatically extracts cell functions and generates optimal vectors required for accurate SPICE characterization of the latest VDSM effects including simultaneous switching.
- .lib noise support for advanced VDSM technologies
Fast & Accurate
- Concurrent timing and power characterization results in near zero overhead for power library generation
- Support of multi-threaded and SUN Grid based environments provides near linear speed-up
- Includes fast API-based SmartSpice characterization engine with 100% HSPICE and SPECTRE compatibility for all public models
- Supports HSPICE, SPECTRE and ELD0 as external simulators
- Automatic vector sizing option for optimal SPICE characterization run-times

Timing
Optimizable slope and load tables for timing arcs.

Power
State-dependent power analysis considers all power effects.

Flexibility & Industry Standard Output
- Flexible simulation bypass, debug and reporting options enable rapid validation of scripting solution and root cause analysis of characterization difficulties
- Generates accurate single-pass, state-dependent timing, power and leakage Liberty .lib libraries
- Automatically generates Mentor ATPG format test library
- Selectable and customizable verilog modeling options for support of various simulator and regression / back-annotation verification methods
- Automatic HTML cell library datasheet generation. Datasheet includes: optional AVG power and MAX frequency reporting, optional user schematic, symbol and truth table info, optional physical cell details and cell description sections
- Powerful table-based user defined vector scripting option enables customization of unique characterization requirements
- Flexible characterization and reporting options for optional state-based leakage, switching, hidden and average power analysis
- Support for user defined I-V, glitch, noise immunity and noise propagation options
QA & Validation Capabilities

- Automatically generates verilog testbench with vectors for function verification
- Special audit mode options for advanced access to all run-time info for QA validations
- Graphical .lib viewer for QA analysis and comparison of timing and power result details

AccuCell Inputs/Outputs

- Configuration Files
- Spice Netlists

AccuCell

- Synopsys Liberty™ (.lib)
- Verilog
- HTML Datasheet

SmartSpice

HSPICE

SPECTRE

ELDO

SILVACO

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