AccuCore performs timing characterization of multi-million device circuits with SmartSpice accuracy and performs block and full-chip Static Timing Analysis (STA) on multi-million gate designs.

- Generates Liberty™ (.lib) and .sdf timing models, gate-level verilog netlist, and generates or reads DSPF and .sdf files for STA
- Exports fully sensitized SPICE decks for selected critical paths and clocktrees with measurements
- Automatically partitions blocks into cells
- Automatically extracts cell functions and generates vectors required for accurate SPICE characterization
- Includes fast API-based SmartSpice characterization engine
- Complete block and full-chip gate-level STA environment for rapid bottleneck analysis and timing verification
- Powerful command set enables mixing both custom and ASIC/SoC functions in a single analysis environment
Setup and Scripting Capabilities

- Automated .lib to .cfg import for easy setup and scripting with various .cfg validation options
- Supports full case sensitivity flows
- Supports both flat and hierarchical design flow
- Advanced RC mode for efficient handling of large designs
- Advanced slope propagation and threshold management options
- Supports various user defined loading methods
- Automatic hierarchical and flat netlist partitioning of blocks to cells with advanced user override options
- Dedicated RAM/CAM partitioning with sense amp and read/write cycle options
- Advanced strength and state-based function extraction features
- Automatic clock propagation with advanced user overrides
- Supports user defined input vector constraints
- Advanced debugging and design reporting options for quick root-cause analysis

AccuCore Block Characterization and Modeling with STA

- Includes fast API-based SmartSpice characterization engine (100% HSPICE and SPECTRE compatible)
- Cell matching improves reuse and incremental update capabilities
- FAST_MODE option for fast prototyping analysis
- ASIC flow option for easy standard cell-based flows
- Automatic input capacitance characterization method
- Automatic setup and hold, recovery and removal and minimum pulse width characterization and user defined override options
- Automatic vector ordering and sizing with user override
- Advanced one-time multi-corner, multi-mode full path model characterization for fast STA
- Supports direct simulator option control with defaults
- Generates gate-level verilog netlist and timing models with output format options
### Block-level STA Capabilities

- Enables gate-level timing checks of custom transistor level designs
- Utilizes advanced path tracing algorithms of longest and shortest paths
- Performs both critical and sub-critical method tracing to avoid multi-layer timing problems
- Automatic false path elimination
- Numerous path limiting and pin, net and arc based blocking options
- Performs function-based clock and constraint propagation reducing ECO re-analysis ripple-effects
- Supports various design styles of both static and dynamic logic, latches, flip-flops, muxes, and tristate circuits
- Built-in timing checks simplify constraint specification
- Analyzes gated and multi-frequency clocks across multi-cycle paths
- Permits customized gated clock, data-to-data and clock-to-data path timing checks
- Supports DSPF and SDF back-annotation
- Performs bottleneck analysis of arrival and required path net and pin based timing requirements
- Permits separate multiple rise and fall edge timing specifications common in footless logic

### AccuCore Output Files

```plaintext
Example .lib pin timing for one pin of a 64 bit shift block using a 5 x 5 slope/load matrix.
```

### Full-chip STA Capabilities

- Concurrently performs both block-level and full-chip STA
- Generates compressed, ring/interface and blackbox timing models
- Supports hierarchical verilog and mode-based multi-corner analysis
- Supports both DSPF and SDF back-annotation
- Enables constraint management, block-level constraint generation and slack allocation for hierarchical design methods
- Permits user-specified uncertainty and skew relationship driven timing analysis with common path optimization
- Advanced debugging features for clock waveform and clock propagation
- Advanced debugging features for netlist, library and analysis verification
- Tcl API interface for custom reporting and analysis functions