SmartSpice delivers the highest performance and accuracy required to design complex high precision analog circuits, analog mixed-signal circuits, analyze critical nets, characterize cell libraries, etc. SmartSpice is compatible with popular analog design flows and foundry-supplied device models.

- 100% HSPICE™ and SPECTRE™ compatible for netlists, models, analysis features, and results
- Provides the most accurate circuit simulation results for critical analog designs
- A leader in run-time simulation speed among SPICE circuit simulators
- Multiple solvers and stepping algorithms for robust convergence
- Largest collection of calibrated SPICE models for traditional technologies (Bipolar, CMOS) and emerging technologies (TFT, SOI, HBT, FRAM, FinFET, etc.)
- Provides open model development environment and extensive analog behavioral capability with Verilog-A
- Enables SEE (Single Event Effects) reliability analysis for nanometer scale designs
- Silvaco’s strong encryption is available to protect valuable customer and third party intellectual property
- 64-bit support for Windows and Linux to allow larger designs
**Accuracy:**
SmartSpice is the most accurate circuit simulator for critical analog designs incorporating nanometer effects.
- Uses Gaussian elimination in an efficient matrix (based on the original Berkeley 3C1 solver)
- A library of direct and iterative solvers
- Verifies and validates Berkeley physics-based model parameters at run-time for continuity, linearity, and valid parameter range
- Detects inconsistencies in poorly-extracted foundry models and prevents these errors from degrading the final product performance and accuracy
- Offers a full set of options for controlling speed vs accuracy of simulations

**Speed**
- Simulates at 2 to 4 times the raw speed of other SPICE products
- Supports multiple parallel 64-bit CPUs for near-logarithmic multi-threaded operation speed
- Network distributed SmartSpice and remote .ALTER
- Network distributed Monte Carlo analysis
- Effective parallelization using pool of threads

**Convergence:**
SmartSpice selects the right solver for optimal convergence
- Surveys initial conditions and iteratively sequences through a series of methods and algorithms to attain optimal convergence
- Multiple solvers provide the best solver for a given circuit topology and multiple high precision solvers are available

**Analysis:**
SmartSpice offers user-defined support for analysis options
- Stop/Continue Algorithm for transient analysis
- Nested parametric analysis
- Scoping of names used in netlist
- Fast cell characterization via direct matrix access on the next parametric step
- Sophisticated optimization at the sub-circuit level
- SEE analysis using .RAD statement leveraging foundry supplied compact models
- Equation editor for .MODEL parameters to support sub 45 nanometer designs
### Ease of Adoption into an Existing Design Flow:

SmartSpice fits your design flow and foundry models.

- SmartSpice can co-exist in an existing design flow implemented with HSPICE and Spectre.
- Supports foundry-supplied SmartSpice, HSPICE and SPECTRE models.
- Supports legacy netlists from HSPICE, SPECTRE™, and Berkeley SPICE.
- Seamless integration with Cadence analog environment through ADE with SmartSpice run in Spectre compatible mode.
- You can run job submission software (LSF, Sun Grid, etc.) seamlessly.
- Seamless integration with Silvaco PDK-based analog/mixed-signal/RF tool flow.

### Model Development Capabilities:

- Core competence in SPICE modeling, data acquisition and model parameter extraction since 1984 with Utmost for the highest accuracy in analog models.
- Verilog-A models offer fastest method for implementing Accellera standard electric-thermal models, sensor models, and other mixed physical effects. A Verilog A debugger is incorporated to aid custom model development.
- Silvaco offers accurate and prompt SPICE Modeling Services to extract DC, AC, S-parameters, capacitance, temperature, noise, and SPICE parameters over full temperature and corner models using statistical analysis.

### Models Available

<table>
<thead>
<tr>
<th>BJT/HBT</th>
<th>MOSFET</th>
<th>TFT</th>
<th>SOI</th>
<th>MESFET</th>
<th>JFET</th>
<th>Diode</th>
<th>FRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gummel-Poon, Quasi-RC, VBIC, MEXTRAM, MODELLA, HiCUM, HBT, HiSIM-IGBT</td>
<td>Level 1,2,3, BSIM1, BSIM3, BSIM4, BSIM6, BSIM-CMG (FinFET), BSIM-IMG, MOS II, MOS 20, EKV, PSP, HiSIM, HiSIM2, Level 88, HiSIM_HV, HiSIM_HV2, MOSVAR</td>
<td>RPI poly-Si, a-Si TFT, UOTFT, MOTFT</td>
<td>Berkeley BSIM3SOI, BSIMSOI4, CEA/LETI SOI</td>
<td>Stats, Curtice I &amp; II, TriQuint 1, 2 and 3</td>
<td>LEVEL 1, LEVEL 2</td>
<td>Berkeley, Fowler-Nordheim, Philips JUNCAP/Level 500, HiSIM Diode</td>
<td>Ramtron FCAP</td>
</tr>
</tbody>
</table>

### Inputs

- Berkeley SPICE, HSPICE and SPECTRE netlists, W-element RLGC matrix files, S-parameter model files, Verilog-A.

### Outputs

- Rawfiles, Output listings, Analysis results, Measurement data, (portable across UNIX/windows platforms).