Gateway supports flat or hierarchical designs of any technology. Gateway readily accepts legacy designs from other schematic editors through the EDIF 2 0 0 standard. Gateway can be used by large design teams through global preferences and handles multiple designs and technologies with specific workspaces.

- Powerful schematic capture and editor functionality to create and modify multi-view, multi-sheet, hierarchical IC designs
- GatewayViews is licensed at no cost for only viewing and navigating schematic designs
- Seamless integration with SmartSpice Circuit Simulator that creates an interactive design environment with behavioral models, cross-probing, waveform display, and analysis
- Create HSPICE compatible input decks
- Controls multi-user projects with shared work spaces for libraries of cells and symbols used by the design team
- Transition from other schematic capture tools via EDIF 2 0 0
- Create netlists for simulation, NDL and LVS from one schematic
- Silvaco’s strong encryption is available to protect valuable customer and third party intellectual property
Gateway provides a front-end to hierarchical design with cross-probing, marching waveforms, analysis options, and optimization.

- Easy to create symbols, subcircuits, subschematics, and Verilog-A models
- Comprehensive symbol creation and editing features for simulation, schematic-driven-layout, and LVS compatibility
- User-configurable keys for repetitive tasks and to emulate legacy capture tools
- Comprehensive search and replace to process porting, IP reuse, and interactive design
- Hierarchical capture for modular, reusable designs, libraries, and working with legacy circuits
- Powerful edit-in place functions with wires, busses, bus ripping, and bus merging
- Designer configurable rule checks show electrical drawing rule violations and illegal names
- Parameterized cells (Pcells) source design entry data for autogeneration of design-rule-connect layout components

Ease of Use and Adoption

- Easy to use for both new and experienced designers with intuitive left-to-right design approach, tool tips, and batch simulation control
- Easy to set up multi-user environment with libraries and import legacy data using EDIF
- Help functions and tool tips for new users
- Batch mode simulation options directly accessible from schematic
- Parameter minimum/maximum checking eliminates entry errors
- Supports wire to wire, wire to pin, wire by name, and implicit/global connections
Integrated Custom IC Design Platform

- Front-to-back design automation solution for custom analog circuits
- Connects Silvaco behavioral modeling, schematic, circuit simulation layout, DRC, LVS, and parasitic extraction with proven feedback flows
- Integrated with SmartView Graphical Waveform Postprocessor for overlaid measurements of delays, slopes, overshoots, rise-time, and eye diagrams – complete with vector calculator
- Powerful cross-probing between schematic and post-processing provide real-time design feed back
- Call-backs evaluate expressions in real-time for design rules, tolerances, parametric calculation, and process skews
- DC bias display for currents and voltages throughout hierarchy

Gateway provides an environment for mixing transistor and behavioral level (Verilog-A) schematics to minimize design time and maximize efficiency. Verilog-A schematics may be used for behavioral block design or compact model design.

Designer Productivity

- Creates multiple views for layout, simulation, and LVS for design integrity and smooth tapeouts
- Spreadsheet data entry, netlist import, EDIF reader, and automatic symbol generation for easy re-use of legacy circuits
- Supports encrypted netlists behind symbols in design kits for IP distribution
- Marching waveforms allow real-time viewing of simulation results to check on long simulations
- Efficient control of the design flow between schematic, simulation, and analysis
- Highlights errors and zooms to schematic location/level for correction
Gateway applications include interactive IC design to build and port digital and analog blocks, standard cells, I/Os, and, as shown at the right, hierarchical memories.

DC bias for currents and voltages for Hierarchical and flat drawings.

Gateway in Complete Custom IC Design Platform