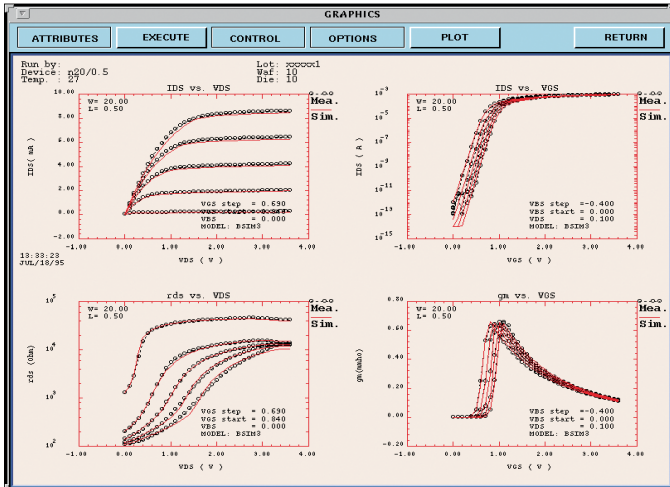


BSIM3v3.2.4

INDUSTRY STANDARD SUB-0.13 MICRON MOSFET MODEL



Simulation of i_{ds} , g_{ds} and g_m demonstrates the model accuracy.

Advanced MOSFET Model for Low-Voltage Low-Current Circuit Design

As device complexity increases and feature sizes shrink into the deep sub-micron region, modern circuit designs require a robust, accurate and computationally efficient MOSFET model. BSIM3v3.2 has been specifically developed for deep sub-micron circuit designs current and future. IC companies and foundries are now rapidly moving past outdated SPICE models and adopting BSIM3v3.2 to meet the challenges of deep submicron designs.

As a public domain standard model BSIM3v3.2 facilitates product design and technology exchanges among foundries and companies.

Silvaco Improvements

- BSIM3v3.2 MOSFET model is part of the SmartLib product-independent model library
- Silvaco implementation is referred to as MOSFET model LEVEL 8 and is based on the version (3.2.4) released by UC-Berkeley on December, 21 2001. It is also possible to invoke HSpice-compatible implementations by setting LEVEL=49 or 53
- Further speed improvements can be gained through the VZERO option and the multi-threading capabilities
- The diagnostics option EXPERT is supported in BSIM3v3 to help the designer find convergence problems
- Parasitic elements are described using SmartSpice Common Equations
- Usual MOS device variables like currents, conductances, charges and capacitances as well as BSIM3v3.2-specific internal variables can be saved, printed, plotted and /or measured
- A stress effect model can be used for process-induced stress, based on BSIM4 implementation

Advanced Physics-Based Model Equations

BSIM3v3.2 uniquely accounts for many of the physical effects present in today's deep sub-micron designs:

- Short and narrow-channel effects
- Non-uniform-doping effects
- Mobility reduction due to vertical field
- Bulk-charge effect
- Carrier velocity saturation
- Drain induced barrier lowering
- Channel length modulation
- Source/drain parasitic resistances

The BSIM3v3.2 model equations account for all of the physical effects listed. Some of the significant benefits to analog designers include:

- Improved threshold voltage model to simulate both short and narrow-channel effects more accurately
- Improved R_{ds} fit provides accuracy and efficiency
- Improved body bias dependence on narrow width, bulk charge effect, drain-induced barrier lowering effects and mobility
- Provides geometry dependence of channel length and width reduction factors
- Includes the drain bias dependence of subthreshold swing
- Accurate substrate current model
- Non-quasi static capacitance model

As seen from this partial list of physical effects, the extreme complexity of the model requires a deep understanding of device physics for proper implementation. Silvaco is the ONLY Spice vendor with this knowledge capable of offering the BSIM3v3.2 model in its full potential to the circuit design community!

Unique Features

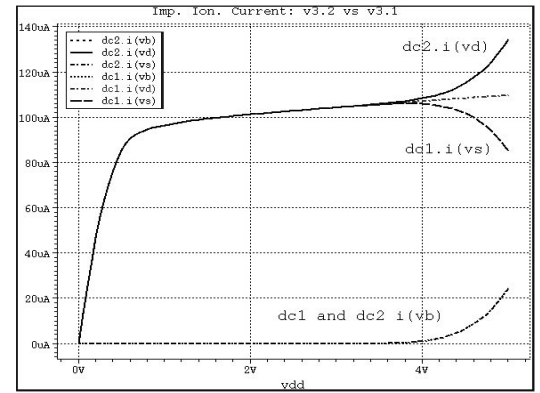
- Physical model based on process parameters
- The physical nature of BSIM3v3.2 provides scalability and accuracy
- Single model provides good fit across all geometries and bias conditions with no binning requirements
- Suitable for both analog and digital applications
- Superb convergence achieved through continuous first and second derivatives

SILVACO

BSIM3v3.2 Fundamental Improvement in SmartSpice

Channel Length Effects on Impact Ionization Current Partitioning

SmartSpice has the most accurate substrate current model available. New parameter (iirat) in the impact ionization current equation in SmartSpice takes into account channel length effects previously ignored in the Berkeley models.



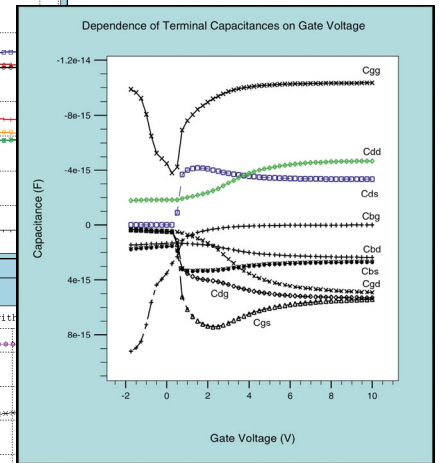
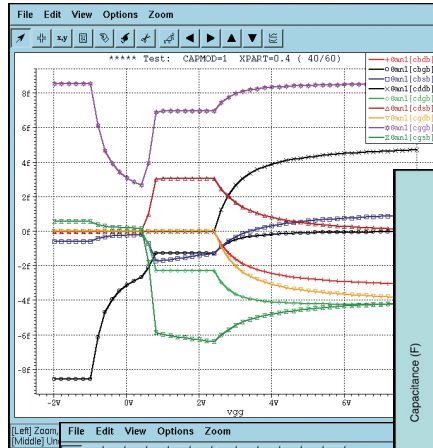
Impact ionization currents in BSIM3v3.2 and v3.1 models.

Correct Intrinsic Capacitance Model

A single capacitance model equation supports effective channel lengths to below 0.2mm. The SmartSpice BSIM3v3.2 implementation eliminates negative capacitance and discontinuity problems found in the Berkeley model. A new parameter (intcap) enables users to choose either the original Berkeley model or Silvaco's advanced implementation.

Improved Non-Quasi-Static Model

A new SmartSpice non-quasi-static capacitance model (inqsmod=5) is physically consistent with the quasi-static model in all operating regions. To model MOSFET devices the nqsmode=5 model, rather than nqsmode=1, is recommended.



Negative capacitances present in the Berkeley BSIM3v3 model (upper-left).

S-Pisces simulation depicts no negative capacitances (upper-right).

SmartSpice BSIM3v3 implementation displays correct model (lower-left).

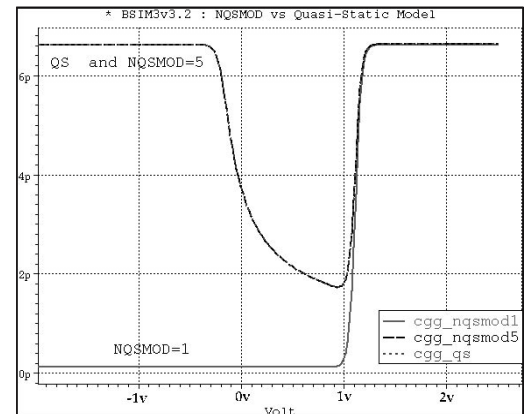
Industry Leading Performance

Silvaco's BSIM3v3.2 implementation contains none of the discontinuities and non-physical behavior found in the original Berkeley model. This results in superior convergence and speed performance surpassing Level 8.

Further speed improvements can be gained through the multi-threading parallelization capabilities available in SmartSpice.

TCAD-Based Implementation

The advancements made in SmartSpice BSIM3v3.2 were made possibly only by utilizing the physics knowledge gained through years of development of the numerical device simulator S-Pisces. Silvaco's BSIM3v3.2 is the only calibrated physical MOS model available!



Total gate capacitance for NQSMOD=1 and 5 models only calibrated physical MOS model available!