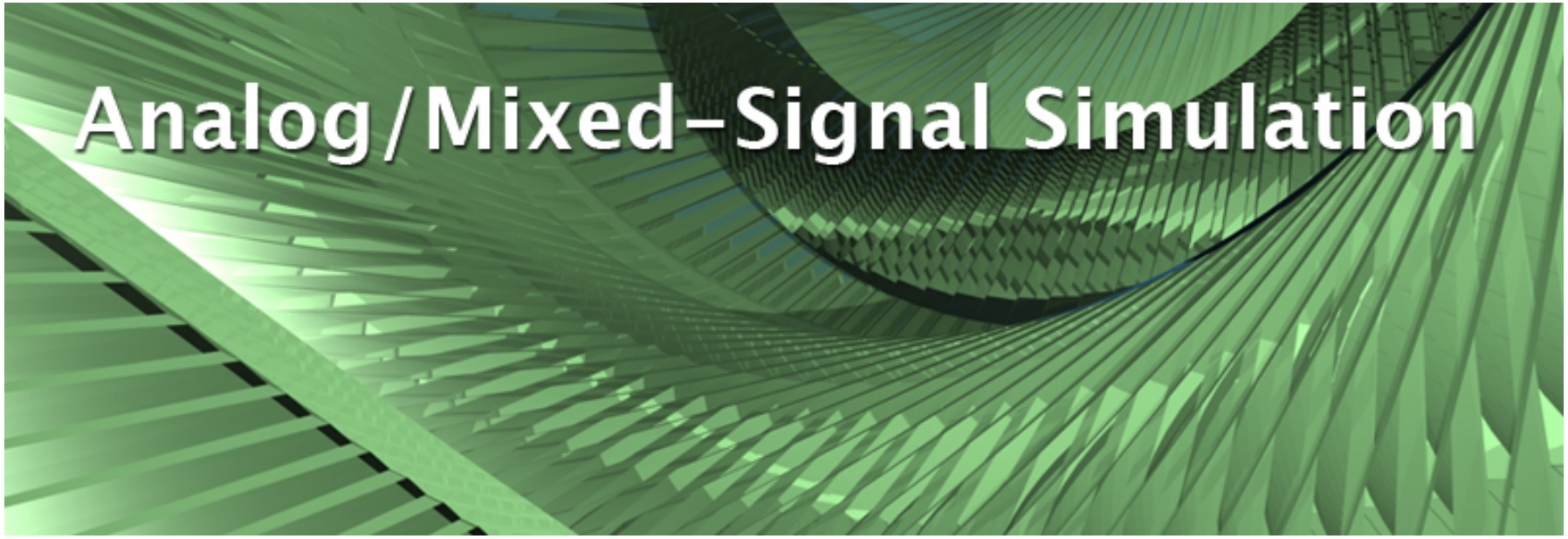
SmartSpice Analog Circuit Simulator



General Overview

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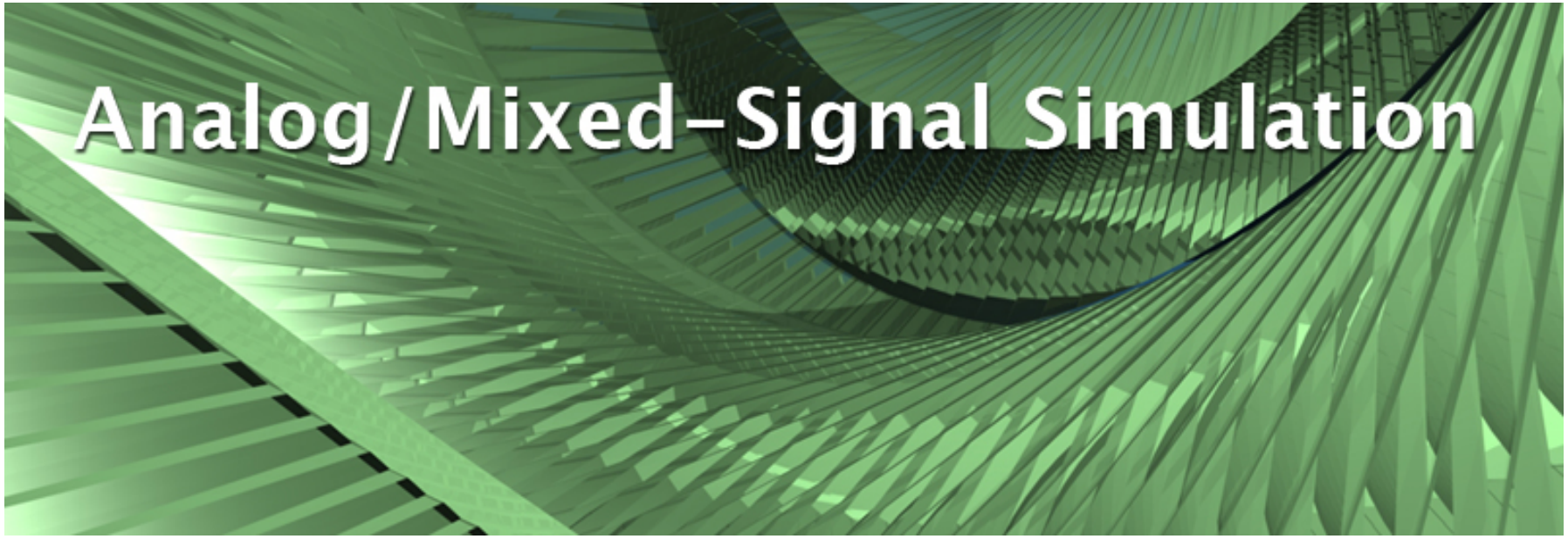
Introduction

- Fast, robust and easy-to-use analog circuit simulator
- Provides industry leading device model technology coverage, simulation speed, convergence and accuracy
- HSPICE™ compatible input decks and translation from the major SPICE products PSPICE™, ELDO™ and Spectre™ with minimal changes
- Has advanced features such as SmartView waveform viewer, interactive run control and industry leading parametric analysis features
- A user friendly interactive interface as well as a batch mode enable both the novice and the experience user to get the maximum from the tool

SmartSpice



General Features

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SmartSpice Analysis Techniques

- DC Analysis
- AC Small Signal
- Transient Analysis
- Transfer Function
- Network Analysis
- Sensitivity Analysis
- Noise Analysis
- Transient Noise Analysis
- Distortion Analysis
- Fourier Analysis
- Forward/Reverse FFT
- Monte Carlo Analysis
- Worst-Case Analysis
- Pole-Zero Analysis

Parametric Analysis Statements

- What is Parametric Analysis?
  - Parametric analysis commands allow the user to completely characterize the behavior of the circuit by varying the IC fabrication and operating environment parameters
- Why is it important?
  - Creates an environment in which users can rapidly change parameters and test conditions to stress designs under real-life conditions. This insures the reliability of the circuit design

Parametric Analysis Statements (con't)

- Any device or model parameter can be printed, plotted or measured
- Any device, model or output statement can be parametrized using parameter labels defined by the user in .PARAM statements, on .SUBCKT and X-Cell lines. Parameter labels and parametric expressions can be used anywhere in the input deck
- Any device or model parameters can be modified by parametric analysis commands during simulation
- The reserved parameter label M can be used to specify devices or subcircuits connected in parallel
- Any voltage or current vector, any device or model parameters can be measured by .MEASURE statement

Parametric Analysis Statements

1 - Global Parametric Analysis Commands:

- SmartSpice supports global and local parametric analysis statements. Parameter modifications made by a global command are applied to the entire input deck. Global parametric analysis commands are:
  - .MODIF - Parametric Analysis Statement
  - .ALTER - Alter Input Deck Statement
  - .TEMP - Temperature Statement

.MODIF Statement

- The .MODIF statement is the most powerful parametric analysis statement in SmartSpice
- This statement can simultaneously and independently modify any device, model parameters, user-defined parameters, temperature and control options
- It terminates the parameter modification process when the user defined stop conditions are satisfied
- Monte Carlo analysis can be performed by the .MODIF statement using 8 types of built-in distribution functions
- Circuit performance measure optimization, and function optimization are based on the .MODIF statement

.MODIF Statement (con't)

Example on using .MODIF :

```
.MEASURE     TRAN     DELAY_OUT     WAVE     V(OUT)
.MODIF       RC1(RES) = 2K          CLOAD(CAP) = 0.5PF
+ MODIF     LOOP =9     STOP     DELAY_OUT    LE   1.3ns
+ RC1(RES) * = 0.9          CLOAD(CAP) * = 0.95
```

- SmartSpice performs nine or fewer iterations
- In the first iteration it sets the parameters RES to 2K and CAP to 0.5pF
- On each of the following iterations, it multiplies RES by 0.9 and CAP by 0.95 until the measured value DELAY_OUT is less than or equal to 1.3ns

.ALTER Statement

- The .ALTER statement is used for modifying and reloading the input deck several times to
  - alter the model libraries,
  - alter or modify subcircuit definitions,
  - add new analysis commands,
  - modify or add new output statements,
  - modify or add new parameter labels,
  - modify parametric analysis commands,
  - modify or add new control options.
- The . ALTER statement is particularly efficient in conjunction with the .MODIF statement

.ALTER Statement (con't)

- Example using .ALTER:

```
-
-
-
m1      1       2       0       4       NMOS1       l=20u       25u
-
-
-
.ALTER
m1      1       2       0       4       NMOS1       l=16u       25u
```

- The input deck is loaded twice and two circuits are created
- Two output files are created

Parametric Analysis Statements

2 - Local Parametric Analysis Statements:

- Local commands are locally applied to certain analysis statements such as .TRAN, .DC or .AC.
- Local parametric analysis commands are:
  - .MC - Monte Carlo Analysis
  - .WCASE - Worst-Case Analysis
  - .ST - Nested sweep can be used with the local MODIF (DATA) parameter sets

Monte Carlo Analysis

- The .MC and .WCASE commands perform statistical and worst/best case analyses on the circuit for the specified analysis type
- Monte Carlo analysis can be performed using the . MODI F statement and the . MC statement:
  - Using the . MC statement, Monte Carlo analysis will only be performed on model parameters with user-defined tolerances
  - The .MODI F statement will perform Monte Carlo analysis on parameters defined on the .MODI F statement line, and on model parameters with user-defined tolerances

Monte Carlo Analysis (con't)

- Tolerances for each device or all devices can be defined in the .MODIF statement
  - ALL generates the same parameter values for all devices of the model (100% correlation)
  - EACH independently varies model parameters for each device of the specified model (0% correlation)

.ST Statement

- The nested SWEEP command is locally applied to the analysis statement where it is specified
- The nested SWEEP specification can reference a parametric inline .DATA statement
- A .DATA statement can contain an arbitrary number of sets of parameter values

.ST Statement (con't)

- Example:

  .ST DEC QNL(BF) 10 100 10

- The parameter BF is swept logarithmically from 10 to 100 with a step of 10 points per decade

Parametric Analysis Statements: Conclusion

- Parametric analysis environment in SmartSpice allows the user to be time-efficient because it shortens design cycles. It also insures design reliability by using efficient methods to evaluate the circuit under user-defined conditions

Problem Diagnostics

- The SmartSpice diagnostics help the designer to rectify a problem in a timely manner
- SmartSpice offers very powerful internal diagnostics based on the EXPERT option. The diagnostic information assists designers with any convergence problems that occur during simulation
- The EXPERT option detects:
  1. Possible problems in the netlist, e.g. nonconvergent nodes and devices
  2. Nonphysical and unrealistic device and model parameter values.
  3. Discontinuities in the model equations.
  4. Unrealistic bias conditions during simulation.

Useful .OPTIONS Statements

- VZERO
  - Define the modified nodal analysis(MNA) formulation in SmartSpice .OPTIONS VZERO=2 is recommended when simulating large circuits.
- RAWPTS
  - Used when a large amount of output data is expected. SmartSpice writes data into the output file every RAWPTS points, e.g. .OPTION RAWPTS=300and can speed up the simulation due to the smaller memory footprints
- FORMAT
  - Provides a compact format for .MEASURE output results

Useful .OPTIONS Statement (con't)

- POST
  - Automatically generate a rawfile without using the -r command line option. If the post option is used without a value, then a value of 1 is assumed. The name of the rawfile is derived from the name of the current input deck with a ".raw" extension.
  - The flag for the POST option:
    1. binary
    2. ascii
    3. single precision binary
    4. XDR binary
    5. XDR single precision
- Now SmartSpice automatically allows for binary ordering differences between platforms without user interaction

Useful .OPTIONS Statement (con't)

- ASPEC
  - If ASPEC option is specified, then the default value of the SCALE and SCALM is 1.0e-6, e.g.

    .OPTIONS ASPEC
- POSTRAWPTS (PRPTS)
  - This option allows post-processing when using RAWPTS option .OPTION rawpts=300 prpts
- TMAX
  - Set the maximum internal time step e.g.

    .OPTIONS TMAX=5N

Command Scripts

- The syntax for a command script is:

```
Explanatory Title
.CONTROL
<SmartSpice commands>
.ENDC
```

  - The body of the script can contain any command including calls to other script files
  - Script files use the same syntax as C-shell scripts
  - Supported structures include: foreach, while, repeat, dowhile, if-else-then, label, goto, continue and break

Command Scripts (con't)

- Script_Example

```
.CONTROL
      setplot tran3
      measure max_v1  max v(1)
      measure max_v2  max v(2)
      set numdgt = 12
      echo "The maximum value of v(1) is " $max_v1 > out.$$
      echo "The maximum value of v(2) is" $max_v2>>out.$$
      shell  cat  out.$$
      shell rm  out.$
$
.ENDC
```

Command Scripts (con't)

- These features allow the user to generate complex scripts to automate the simulation and analysis process
- SmartSpice also fully supports standard I/O redirection operators and backquote substitution which allows shell commands to be evaluated and the results to be assigned to internal SmartSpice variables
- This allows importing a results file and extracting more data without the time penalty of re-running the simulation

Batch Mode Operation

- Source input deck.
- Parse devices, models and statements
  - Warnings will be printed if parameters/options are not understood, expressions are invalid, etc.
- Execute analysis statements or execute commands in a .CONTROL … .ENDC block
- Execute post-processor statements, e.g. .SAVE, .PRINT, .LET, .MEASURE,.GRAPH, .PROBE.
- Save data in a rawfile, if required.
  - Using -r command-line option, or post deck option

Generate Rawfile

- If the -r rawfile command-line option is specified, then all vectors mentioned in post-processor statements will be saved in the rawfile, e.g.

  % smartspice -b filename.in -r filename.raw

- If POST option is used, then the rawfile will be generated automatically, e.g.

  % smartspice -b filename.in

  would generated the rawfile "filename.raw", if post is specified

Optimizer

- The Optimizer is a general purpose optimizing engine that requires initial and target parameter values to be set. The optimizer then iterates these parameters until the target values are reached
- The optimizer provides a comprehensive interface and an interactive display system for visualizing the optimization process as it is executed
- There are no restrictions on the type of circuit analysis that can be performed. Circuits can be optimized in steady-state, frequency, and time domains

Optimization Example

- This example shows how to use the optimizer to select the transistor widths of M1 and M2, so that the trip point can be set to 1.55V,with a maximum current through the inverter of 1.9mA
- The trip point and the maximum current values are known as the optimizer targets
- The widths of the transistors are known as the optimization parameters

Convergence and Speed

- SmartSpice provides superb convergence and speed because of:
  1. Advanced convergence algorithms
  2. Initial points algorithms
  3. Options and advanced timestep control algorithms to speed up simulation
  4. Model continuity
  5. Comprehensive problem diagnostics
- Customer benchmarks have demonstrated 8 times speedup over other major circuit simulators for large circuits containing thousands of transistors

Convergence and Speed (con't)

- Convergence
  - Superior convergence is achieved through much better solvers and numerical techniques and much better models resulting from years of R&D
  - Large and complex circuits are easily handled with SmartSpice
- Speed
  - Superior speed against all other Spice vendors for single CPU simulation even before introducing parallelization

Convergence and Speed: Convergence Algorithms

- DC convergence is based on proprietary stepping algorithms developed by Silvaco
- The option CONV=5 (default) helps the Newton-Raphson method to find a solution starting from (typically) zero initial conditions
- To achieve DC convergence it automatically selects one of the following advanced stepping algorithms:
  - GMIN stepping
  - DiagGMIN stepping
  - DCGMIN stepping
  - Source stepping
- The proprietary Transient Ramping Algorithm is used in the most difficult cases to compute steady state solution

Convergence and Speed: Problem Diagnostics

- SmartSpice offers very powerful internal diagnostics based on the EXPERT option
- The diagnostic information assists designers with any convergence problems that occur during simulation

Convergence and Speed: Options

- A number of options are supported in SmartSpice to detect possible model problems and increase the simulator performance
- The most important options are:
  - EXPERT
  - VZERO

Convergence and Speed: Options (con't)

- Option EXPERT
  - The option EXPERT is supported in all models. The option EXPERT can be used to detect, before and during simulation, possible problems in models such as:
    - negative conductances GM, GDS and GMBS
    - negative capacitances
    - active smoothing functions
    - positively biased bulk to drain or bulk to source diodes
- Option VZERO
  - The option VZERO=2 is recommended when simulating in the time domain relatively large circuits with hundreds and thousands of transistors. It accelerates simulation and increases accuracy of simulation results.

Parallel SmartSpice

- Other Approaches to Speed Up Circuit Simulation?
  - Methods used in timing simulation:
    - Table Lookup Methods
    - Event-driven simulation
    - BOTH METHODS LEAD TO A LOSS OF SPICE ACCURACY
- Silvaco's Approach: Parallel SmartSpice
  - Retains all spice advantages:
    - Arbitrary circuit geometries
    - Analog / Digital
    - Same accuracy in Silvaco's implementation as SmartSpice
    - Multi processor capability to increase throughput

Parallel SmartSpice (con't)

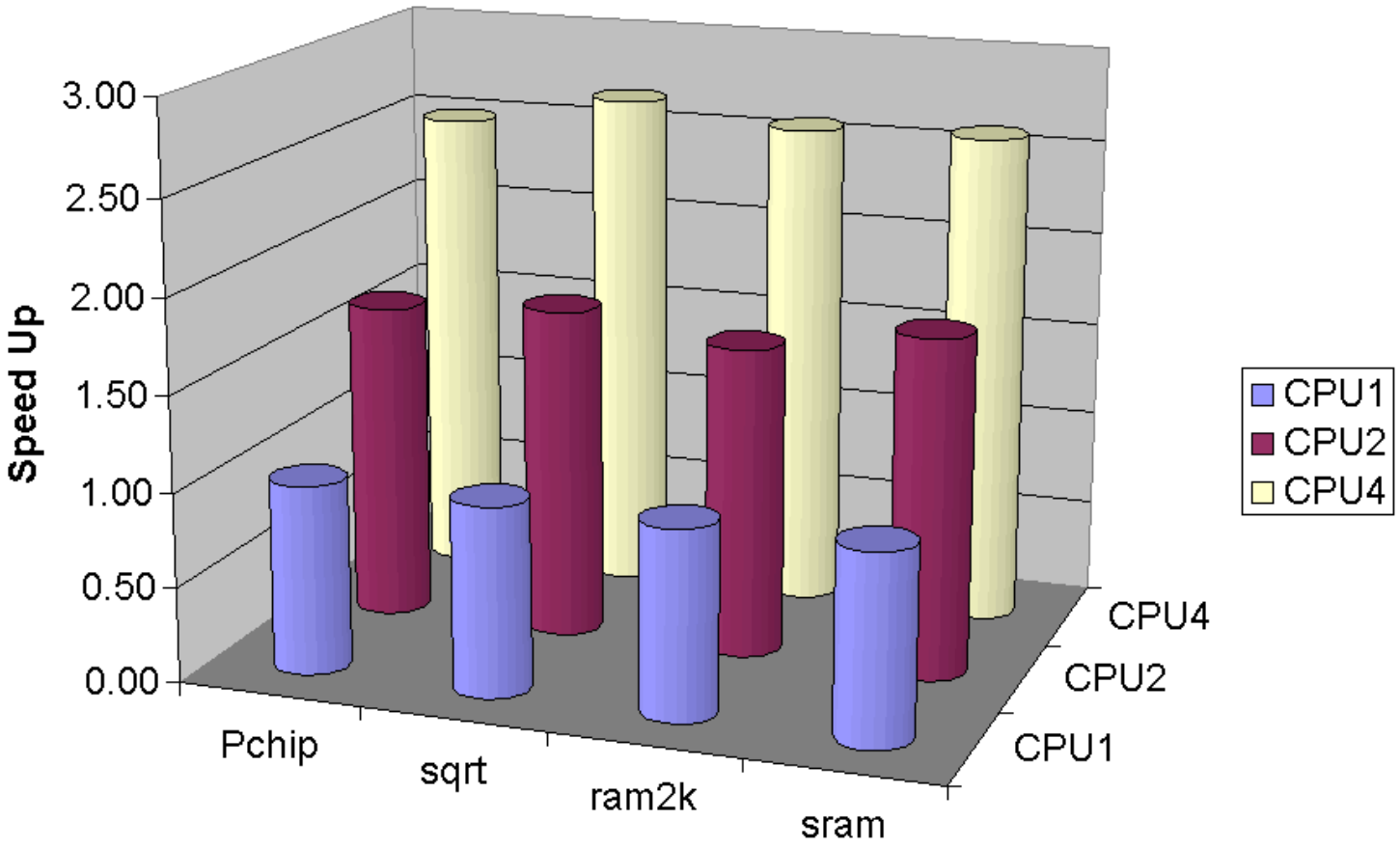
- Parallel SmartSpice features state-of-the-art parallelization techniques:
  - Parallel model evaluation:
    - Automatic circuit/task partitioning
    - Automatic Job Scheduling and processor mapping
    - Blocking and Caching for limited interprocessor synchronization overhead
    - Support of all models
  - Parallel Linear Solver:
    - Column-based task partitioning
    - Elimination tree-based level scheduling
    - Event-based Synchronization

Parallel SmartSpice (con't)

- Plus:
  - Speeds Up the simulation
  - Larger circuit sizes thanks to large amount of memory in parallel computers
  - No user partitioning required
  - The models remain virtually the same
  - No calibration required
  - No extra user intervention

Only prerequisite: a Parallel Computer (shared memory desktop /desk-side)

Parallel SmartSpice - Linux



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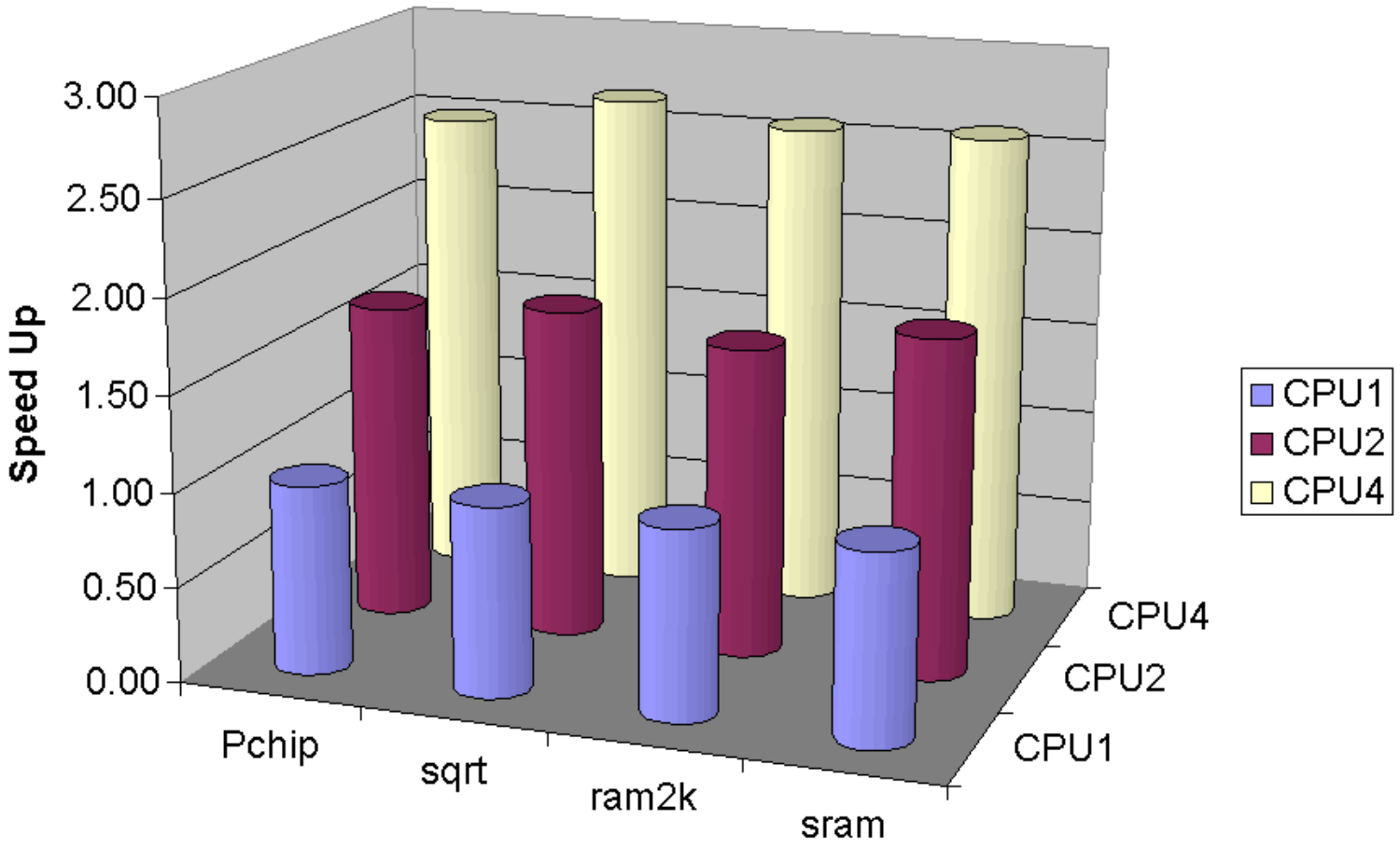
Parallel SmartSpice - Windows



HSpice™ and PSpice™ Compatibility

- SmartSpice uniquely offers compatibility with HSpice and PSpice that:
  - Preserves past investment
    - Designs completed using HSpice and PSpice can be re-simulated without modification
  - Reduces design inefficiencies and internal support requirements
    - Single fully-supported Spice vendor allows companies to focus on design

HSpice™ and PSpice™ Compatibility (con't)

- Creates new freedoms
  - Site licenses, enhanced models, superior features and analysis capabilities
- Makes Replacement Simple
- Silvaco is the ONLY Spice vendor that offers and continually supports compatibility

HSpice™ and PSpice™ Compatibility (con't)

- To summarize:
  - Backward compatibility is essential for smooth transition from existing Spice simulator to an improved Spice Solution
  - Preserves past investment
  - Provides new capabilities

Platform Compatibility

- Identical Code available on both Windows 2000/XP, UNIX and Linux
- SmartSpice provides the ONLY available high performance Spice solution to meet the needs of analog designers as Linux emerges as a significant design platform
- Platform compatibility allows netlists to be simulated on either UNIX or PC platforms providing portability of designs across facilities or between home and work

Integration with Leading CAD Vendors

- Cadence - SmartSpice Integration
  - Tight coupling with Analog Artist 5.0, 5.033, 5.1.41 through OASIS interface
  - Includes Mixed-Signal simulation with VeriLog
  - Supports cross-probing and back annotation of simulation results
  - Seamless integration offering an additional more powerful SPICE engine without significant disturbance to the user environment and controls

SmartSpice Interpreter

- Allows user-defined models to be quickly and simply added to SmartSpice using C language syntax
- Powerful interactive debugger facilitates development / verification of new models
- Allows new models to be compiled into dynamic libraries which execute very quickly
- Provides extensive interface functions to SmartSpice internal data structures and procedures
- Very suitable for collaborative model development between Silvaco and its partners

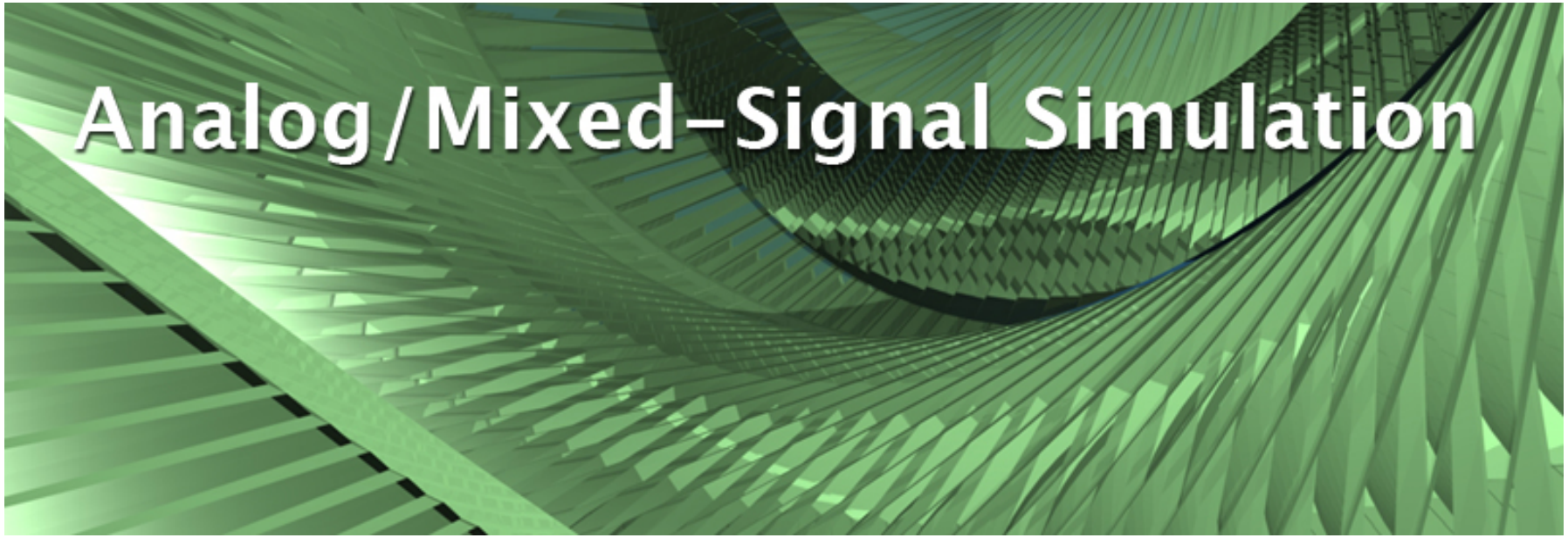
Searching a Model Library

- It is not possible to cover wide ranges of device sizes with a single model
- Search model library based on the width and length of the MOSFET (Binning)
- Parameters WMIN and WMAX, LMIN and LMAX set the range for the model selection based on the device width and length
- A continuous model approach to get a greater model flexibility. This allows the simplicity of a single model approach with greater accuracy then the binning method

SPICE Modeling Services

- Modeling Service provides cost effective, fast turnaround and high quality models and is an alternative for many companies
- Suitable for new model evaluation
- Services Include:
  - Extraction of DC, AC (s-parameters), Capacitance, Temperature, Noise and SPICE parameters
  - Packaged parts or wafers are acceptable
  - Temperature range from –55C to + 150C
  - All commercially available SPICE models supported
  - Model validation in accordance with Fabless Semiconductor Association (FSA), Compact Modeling Council, and IEEE test procedure #P1485 recommendations
  - Worst case and corner model generation based on SPAYN

SmartSpice



Device Models

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Device Models

- Comprehensive and up to date set of Intrinsic Device Models
  - MOSFET
    - BSIM1, BSIM2, BSIM3v2, BSIM3v3, BSIM4, BSIM5
    - Philips MOS11 and MOS20, EKV, HiSIM
    - User Models
  - Bipolar
    - Modified Gummel-Poon, Quasi-RC
    - Mextram, VBIC, HICUM
    - Macro Models to include parasitic device effects
    - User Models
- TFT
  - Amorphous and Polysilicon TFT
- MESFET
  - Statz, Curtice I & II, TOM, TriQuint
- SOI, HBT, FRAM, JFET, Diode

Device Models: MOSFETs

- LEVEL 1: Schichman-Hodges model
- LEVEL 2: Modified Schichman-Hodges model
- LEVEL 3: Semi-empirical model
- LEVEL 4: BSIM1
- LEVEL 7: BSIM3

BSIM3v3 and BSIM3SOI Models

- BSIM3v3 and BSIM3SOI models developed for deep sub-micron circuit designs are:
  - Physically-based, scalable and accurate
  - Suitable for both analog and digital applications
  - Superb convergence
  - Berkeley's latest BSIM3v3 and BSIM3SOI models have been integrated into SmartSpice

BSIM3v3 and BSIM3SOI Models (con't)

- New Capabilities and Models
  - The first working BSIM3SOI Simulator
    - Dynamic depletion model
    - Floating and tied body effects
    - Self-Heating
    - Silvaco Improvements
  - Parallel Windows Version
    - Unmatched performance on multi-CPU PCs

Device Models: MOSFETs

- LEVEL 8: BSIM 3v3 (v3.2.5)
- Physical model based on process parameters
- Provides scalability and accuracy
- Single model provides good fit across all geometries and bias conditions with no binning requirements
- Suitable for both analog and digital applications
- Superb convergence achieved through continuous first and second derivatives

Device Models: MOSFETs (con't)

- LEVEL 14 : BSIM4
  - Accurate model of the intrinsic input resistance for both RF, high-frequency analog and high-speed digital applications
  - Flexible substrate resistance network for RF modeling
  - New accurate channel thermal noise model and noise partition model for the induced gate noise
  - Non-quasi-static (NQS) model, consistent with the Rg-based RF model and consistent AC model, accounting for the NQS effect in both transconductances and capacitances
  - Accurate gate direct tunneling model
  - Comprehensive geometry-dependent parasitics model for various source/drain connections and multi-finger devices
  - Improved model for steep vertical retrograde doping profiles
  - Better model for pocket-implanted devices in Vth, bulk charge effect, and Rout equations

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Device Models: MOSFETs (con't)

- LEVEL 14 : BSIM4 (continued)
  - Asymmetrical and bias-dependent source/drain resistance, either internal or external to the intrinsic MOSFET
  - Acceptance of either the electrical or physical gate
  - Oxide thickness as the model input at the user's choice in a physically accurate manner
  - Quantum mechanical charge-layer-thickness model for both IV and CV
  - More accurate mobility model for predictive modeling
  - Gate-induced drain leakage (GIDL) current model, available in BSIM for the first time
  - Improved unified flicker (1/f) noise model, smooth over all bias regions and accounting for the bulk charge effect
  - Different diode IV and CV characteristics for source and drain junctions
  - Junction diode breakdown with or without current limiting
  - Gate dielectric constant defined as a model parameter

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Device Models: MOSFETs (con't)

- LEVEL 55 : BSIM5
  - Built on the well-proven BSIM4
  - Improvements with regard to previous BSIM3v3 and BSIM4 :
    - Fully physical and symmetric
    - Improved reciprocity (no negative capacitances)
    - Better model for moderate inversion region

⇨ Better core using as much as possible of BSIM4 features

Device Models: MOSFETs (con't)

- LEVEL 11: Philips MOS11 model
  - Dedicated to analog, RF and digital simulation
  - Physics based
  - Based on surface potentials
    - Accurate transition from weak to strong inversion
    - Single equation for the whole operating range
  - Symmetrical
  - Good distortion behavior (accurate description of high-order derivatives)

Device Models: MOSFETs (con't)

- LEVEL 20: Philips MOS20 model
  - High-Voltage MOSFET model
  - Especially developed to describe LDMOS, EPMOS and VDMOS models
  - Acts as a replacement of the couple MOS9+MOS30
  - Includes the following effects:
    - Surface potentials computation avoiding smoothing functions between operating regimes
    - Mobility reduction
    - Velocity saturation
    - Drain-Induced Barrier Lowering (DIBL)
    - Static feedback
    - Channel length modulation
    - Weak avalanche current

Device Models: MOSFETs (con't)

- LEVEL 44: EKV MOSFET model
  - Simulation of low voltage, low current analog and mixed signal circuits using submicron CMOS technologies
  - EKV model equation is based on single expression, preserves continuity of first and higher order derivatives
  - Includes the following physical effects:
    - Effects of doping profile, substrate effect
    - Modeling of weak, moderate and strong inversion behavior
    - Modeling of mobility effect due to vertical field
    - Short channel effects for velocity saturation, channel length modulation (CLM), source and drain charge-sharing (including for narrow channel widths), reverse short-channel effect (RSCE)
    - Modeling of substrate current due to impact ionization
    - Quasi-static charge-based dynamic model
    - Thermal and flicker noise modeling

Device Models: MOSFETs (con't)

- LEVEL 88: High voltage MOSFET model
  - Forward and reverse mode of operations
  - Asymmetry of all parasitics (diodes and resistances)
  - Bias dependence of external resistances RDS
  - Dependence mobility degradation on Vds
  - Bias dependent VSAT
  - Transconductance Gm reduction in saturation at high Vds

HiSIM MOSFET Model

- HiSIM version 1.2.0
- Computes surface potentials, from the drift-diffusion approximation
  - No parameter inter-dependence
  - Easy parameter extraction
  - Low number of parameters
  - Continuity of derivatives
  - One parameter set for all channel lengths

Device Models: MOSFETs

- LEVEL 111: HiSIM MOSFET model
- Computes surface potentials, from the drift-diffusion approximation
  - No parameter inter-dependence
  - Easy parameter extraction
  - Low number of parameters
  - Continuity of derivatives
  - One parameter set for all channel lengths

Device Models: BJTs

- LEVEL 1: Modified Gummel-Poon model
- LEVEL 2: Quasi RC (quasi-saturation) model

Device Models: BJTs (con't)

- LEVEL 5: VBIC model versions 1.1 and 1.2
  - Improved early effects modeling
  - Quasi saturation modeling
  - Inclusion of parasitic substrate transistor
  - Inclusion of parasitic overlap capacitances
  - Weak avalanche modeling
  - Improved temperature modeling
  - Decoupling of base and collector currents
  - Electrothermal (self-heating) capability
  - Improved heterojunction bipolar transistor modeling

Device Models: BJTs (con't)

- LEVEL 500: Philips MODELLA model
  - Temperature effect
  - Charge storage effects
  - Excess phase shift for current and storage charges
  - Substrate effects
  - High-injection effects
  - Build-in electric field in base region
  - Bias-dependent early effect
  - low-level non-ideal base currents
  - Hard and quasi-saturation
  - Weak avalanche
  - Hot carrier effects in the collector epilayer
  - Explicit modeling of inactive region

Device Models: BJTs (con't)

- LEVEL 504: Philips MEXTRAM model 504.5
  - Self-heating feature
  - Modelling of SiGe devices, using a dedicated set of parameters
  - Reviewed set of parameters to make extraction procedure easier
  - Smoothed first and higher order derivatives, resulting in better accuracy and convergence

Device Models: Diodes

- LEVEL 1: Standard junction diode model (non geometric model)
- LEVEL 2: Fowler-Nordheim diode model
  - Created as metal-semiconductor or s-m-s
  - The insulator of this type of diode is very thin (about 100 Å), which allows for the tunneling of the carriers
  - Modeling electrically-alterable memory cells and other insulation breakdown devices
  - In many applications, they are in parallel together. The multiplier M is then used to simplify the simulation

Device Models: Diodes (cont)

- LEVEL 3: Junction diode model (geometric model)
- LEVEL 9: Philips JUNCAP diode model
- LEVEL 500: Philips LEVEL 500 diode model
  - Forward biasing (ideal current, non ideal current including tunneling)
  - Reverse biasing (Trap assisted tunneling, Shockley-Read-Hall generation, band-to-band tunneling, avalanche multiplication)
  - Breakdown
  - Series resistances
  - Charge storage effects
  - temperature scaling rules
  - Noise model for RS and the ideal forward current

Device Models: Diodes (cont)

- LEVEL 4: RPI VCSEL laser diode
  - Vertical Cavity Surface Emitting Laser
  - Mixed Electronic/Photonic (MEP) simulation : photonic part described in terms of equivalent electrical signal.
  - Can be connected to transmission line and optical receiver devices

Device Models: JFETs

- LEVEL 1: Basic SPICE model with Sydney University enhancements
- LEVEL 2: Modified SPICE model with gate modulation of LAMBDA
  - Takes into consideration the dependence of channel length modulation on gate voltage (by means of the model parameter LAM1)

Device Models: MESFETs

- LEVEL 1: JFET model
- LEVEL 2: Statz model
- LEVEL 3: Curtice model
- LEVEL 4: Curtice-Ettenburg model
- LEVEL 5: TriQuint model
- LEVEL 6: Parker Skellern model
- LEVEL 7: TriQuint-2 model

Passive Elements and Independent Sources

- Resistors
- Capacitors
- Inductors
- Mutual inductors and magnetic cores
- Switches
- Independent voltage, current, DC, AC, transient or mixed sources

Transmission Lines

- Lossless Transmission Line
- Berkeley Lossy Transmission Line Model
- Lossy Transmission Line - Recursive Convolution Model
- W Element - Multiconductor Lossy frequency Dependent Transmission Line (Under development)

Analog Behavioral Modeling

- Analog Behavioral Device
  - Unique SmartSpice device
  - The current through/voltage across can be an arbitrary mathematical expression referencing node voltage and device current
  - The expression can contain the derivative operator
  - Expressions can contain if…then…else conditions
  - Expressions can access the circuit temperature, current, time and current timestep(tstep)
  - Delay-type device can be used to model an ideal delay

Controlled Sources

- Voltage Controlled Voltage Source
- Current Controlled Current Source
- Voltage Controlled Current Source
- Current Controlled Current Source

SOI Models

- Currently support 6 SOI device models
  - University of Florida, Fully and Partially Depleted SOI models
  - University of California, Berkeley BSIM3SOI models

SOI Model Objectives

- Dynamic depletion is applied on both I-V and C-V. Charge and Drain current are scaleable with Tbox and Tsi continuously
- Supports external body bias and backgate bias; a total of 6 nodes
- Real floating body simulation in both I-V and C-V Body potential is properly bounded by diode and C-V formulation
- Self heating implementation improved over the alpha version

SOI Model Objectives (con't)

- An improved impact ionization current model
- Various diode leakage components and parasitic bipolar current included
- New depletion charge model (EBCI) introduced for better accuracy in capacitive coupling prediction. An improved BSIM3v3 based model is added as well.
- Dynamic depletion selector (ddMod) to suit different requirements for SOI technologies
- Single I-V expression as in BSIM3v3.1 to guarantee continuities of Ids, Gds and Gm and their derivatives for all bias conditions

SOI Models

- LEVEL 21 : UFS (Florida) SOI model fully depleted:
  - Physically accounts for the charge coupling between the front and the back gates
  - 2-D analysis for the subthreshold region of operation has been added
  - Accumulation of charge in the body has been also added, it can drive dynamic floating-body bipolar effects
  - Accounts for DC and dynamic floating-body effects in all regions of operation

SOI Models (con't)

- LEVEL 25: BSIM3 SOIv1 model derived from BSIM3v3.1
  - Partially Depleted (PD) and fully depleted (FD) devices
  - Dynamic and continuous transitions between PD and FD
- LEVEL 26: BSIM3 SOIv2 fully depleted (FD) model
  - Has improved simulation efficiency and noise modeling
  - Supports external body bias and backgate bias (5 ext nodes)
  - Improved self-heating implementation
  - Single I-V expression as in BSIM3v3 guarantees continuities of Ids, Gm, and Gds and their derivatives for all bias conditions

SOI Models (con't)

- LEVEL 27: BSIM3 SOIv2 dynamic depletion (DD) model
  - The dynamic depletion approach is applied on both I-V and C-V
  - Charge and drain current are scalable
  - same features as in LEVEL = 26

- LEVEL 29: BSIM3 SOIv2 partially depleted (PD) model
  - Real floating body simulation in both C-V and I-V. The body potential is determined by the balance of all the body current components
  - Enhancements in the threshold voltage and bulk charge formulation of the high positive body bias regime
  - An improved parasitic bipolar current model
  - An improved impact ionization current model

SOI Models (con't)

- LEVEL 33 : BSIM3 SOIv3
  - Includes Partially and Fully depleted models
    - PD module identical to BSIM3 SOIv2
    - Improved FD module
    - Ideal Fully Depleted model for strongly FD devices (without floating body effect)
    - Non Ideal Fully Depleted model
    - Automatic selection among the above modes
  - New Gate-to-channel and Gate-to-Source/Drain currents
  - New gate resistances model, including RF

SOI Models (con't)

- LEVEL 32: CEA/LETI model (LETISOI)
  - For modeling the static and dynamic electrical behavior of partially-depleted SOI devices
  - Only uses pure analytical current and charge equations

Silicon-On-Isolator (SOI) Properties

- Total dielectric isolation
- Suppressed latch-up effect
- Integration density enhanced
- Junction capacitance reduced
- Device speed increased

Silicon-On-Isolator (SOI) Properties (con't)

- Radiation hardness
- Consumption reduced
- Leakage current reduced
- Reduction of 2-D effects such as GILD and short channel effect

TFT, FRAM, HBT Models

- SmartSpice supports a number of unusual device models:
  - Amorphous and Poly TFT, Hetrojunction Bipolar Transistor (HBT), Ferro Capacitor
  - HBT model developed at University of California, San Diego
  - Includes self-heating model
  - FRAM model developed in conjunction with RAMTRON
  - VCSEL Laser diode model

Thin Film Transistors (TFT) Models

- Amorphous-Silicon TFT models:
  - LEVEL 15: Modified Leroux model
    - Transport by multitraps
    - Channel length modulation (CLM)
    - Exponential localized states density
    - Temperature dependence
    - Overlap resistance Rc

Thin Film Transistors (TFT) Models

- LEVEL 35: Modified RPI model
  - Unified DC model covers all regimes of operation
  - AC model accurately reproduces frequency dispersion of capacitances
  - Provides automatic scaling of model parameters to accurately model a wide range of device geometries

Thin Film Transistors (TFT) Models

- Polysilicon TFT models:
  - LEVEL 16: Modified U.C. Berkeley SPICE 3E1 model
    - Hot carrier
    - Drain induced barrier lowering (DIBL)
    - Channel length modulation (CLM)
    - Thermal generation
    - Gate induced drain leakage (GIDL)

Thin Film Transistors (TFT) Models

- LEVEL 36: Modified RPI model
  - Guarantees stability and conversion
  - Unified DC model covers all regimes of operation
  - AC model accurately reproduces frequency dispersion of capacitances
  - Provides automatic scaling of model parameters to accurately model a wide range of device geometries

Heterojunction Bipolar Transistor (HBT) Models

- LEVEL 20: UCSD-HBT model
  - Based on the standard SPICE Gummel-Poon model

Conclusion

- A Powerful set of analysis features inside SmartSpice coupled with the ability to import other vendor spice decks
- Sophisticated Convergence algorithms and speed options to allow user configuration to his chosen application
- Proven customer speed improvements over other SPICE simulators and the additional capability to run on multiple CPU's
- Multi-Platform support and consistency for both 32bit and 64bit versions
- Comprehensive set of common and up to date models plus custom capability (BSIM, TFT, HBT, FRAM, SOI, HICUM, VBIC, MAXTRAM etc.)

Conclusion (con't)

- SmartSpice is redefining industry standard for convergence, speed accuracy and user-friendliness
- Powerful parametric analysis statement
- Problem diagnostics engine based on EXPERT and VZERO
- Higher speed is achieved through parallelization without losing accuracy
- Comprehensive coverage for advanced models for MOSFETs, BJTs, TFT, SOI, HBT, MESFETs and many other advanced technologies