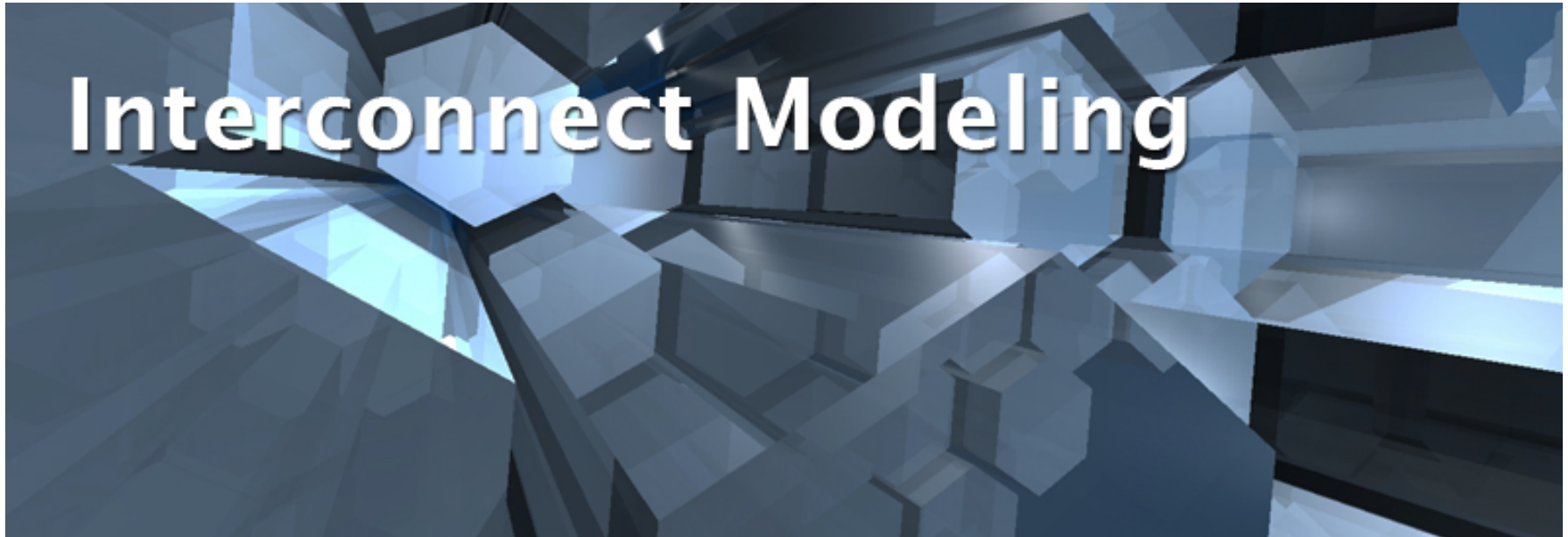


EXACT Interconnect Parasitic Characterization



Application Examples



SILVACO

Interconnect Modeling

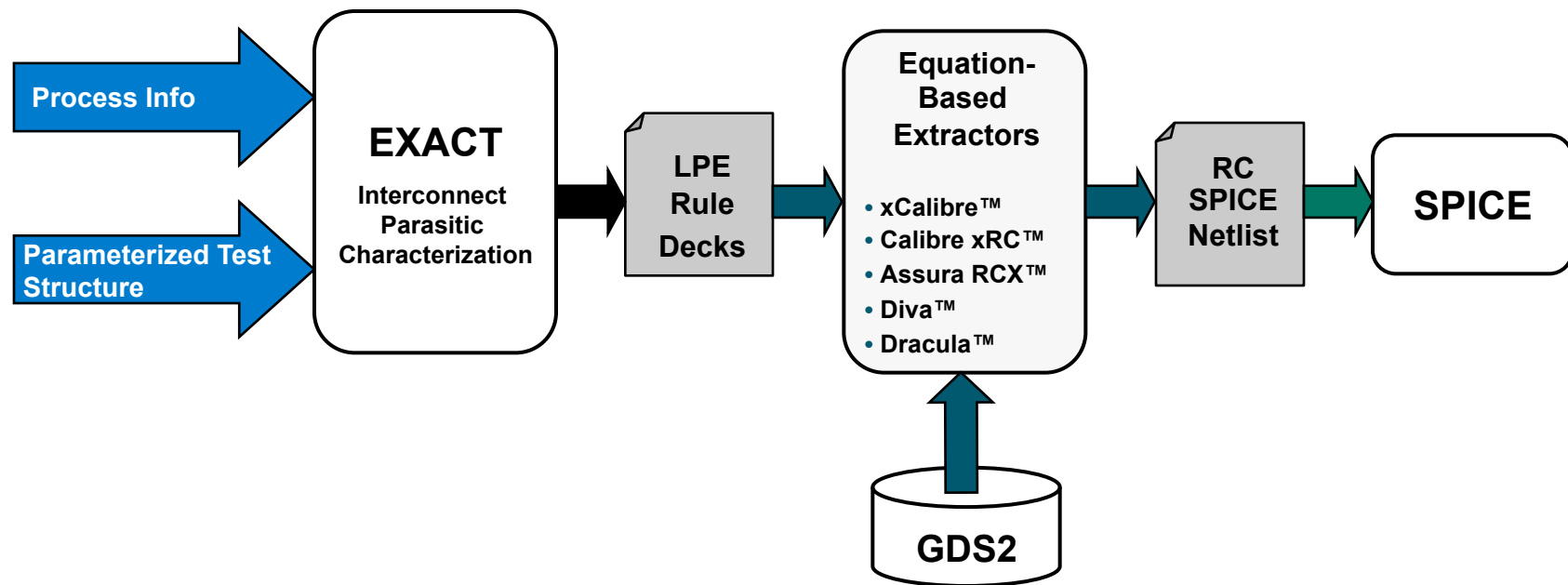
Introduction

- EXACT delivers the most accurate interconnect models for nanometer semiconductor processes and generates layout parameter extraction (LPE) rule files for leading full chip extraction tools
- EXACT's powerful 3D field solvers support xCalibre, Calibre xRC, Diva, Assura RCX, and Dracula LPE

Interconnect Modeling

Introduction: Exact Flow

- EXACT takes process information and produces LPE rule decks



Interconnect Modeling

Introduction: Key Benefits

- Powerful 3D solver supports non-planar semiconductor profiles and dummies
- 3D field solver calculates interconnect capacitance models
- Intuitive and user-friendly graphical interface for process layer description and test structure definition
- Standard mode of operation handles most conventional processes
- Integrated scripting language provides custom LPE rule files for other extraction tools
- Powerful statistical analysis module option available to calculate variations of capacitance

Interconnect Modeling

Introduction: Ease of Use and Adoption

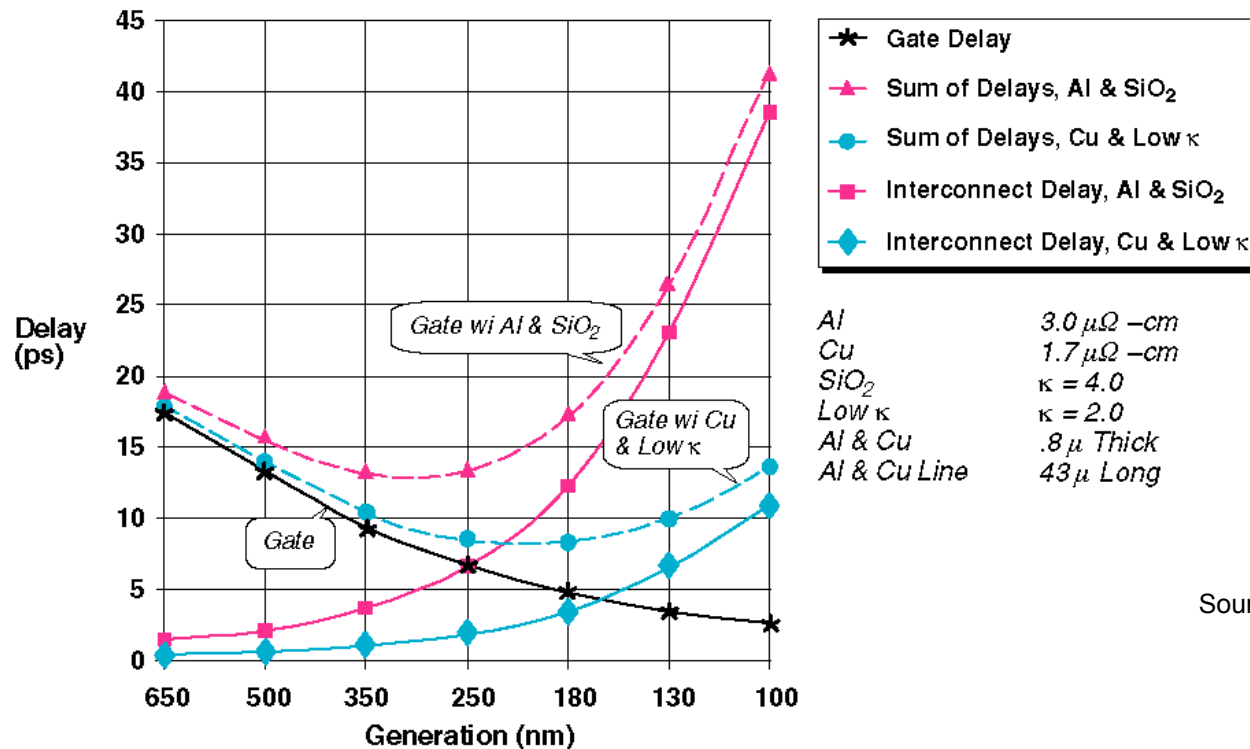
- Easy to use, menu-driven graphical interface for process layer definition
- Menu-driven parameterized layout generator for test structure and pattern generation
- Easy LPE rule generation with LISA™ scripting language
- Flexible architecture for fitting raw parasitic data into a wide range of custom equations for xCalibre/Calibre xRC, and Assura-RCX/ Diva/Dracula LPE
- Easy to understand extracted capacitance tables that facilitate the analysis of effects on interconnect due to various process change or experiment
- Automatic mesh and deck generation and submission to 3D field solver

Interconnect Modeling

Introduction: Importance of Accurate Parasitic Extraction

- Parasitics now dominate circuit timing

SPEED / PERFORMANCE ISSUE *The Technical Problem*

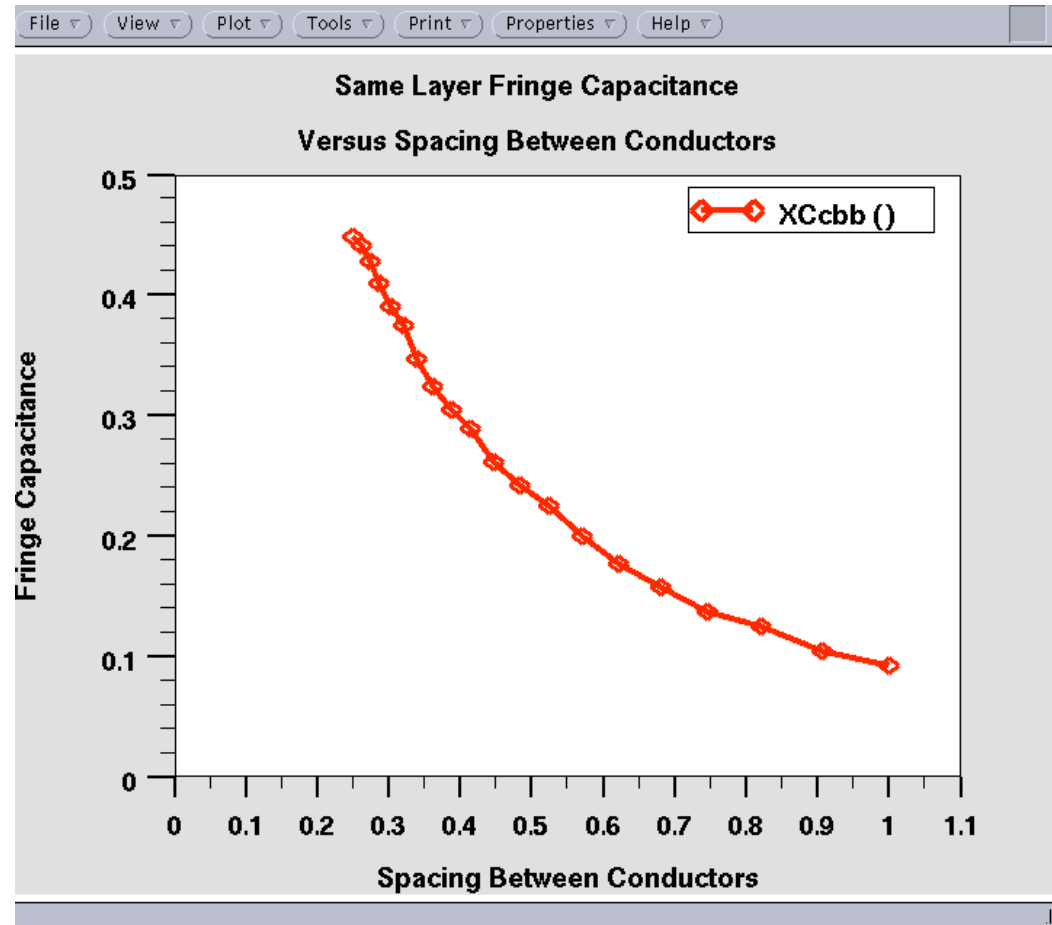


Source: SIA Roadmap 1997

Interconnect Modeling

Introduction: Data Required for Deep Sub-Micron Designs

- Lateral capacitance plot versus spacing between two conducting lines
- The figure shows that in this simple case, the capacitance can vary by a factor of 4 between minimum spacing and only 1 micron away.
- Typical foundry data above would only provide the first point on this graph



Interconnect Modeling

Introduction: Data Required for Deep Sub-Micron Designs (con't)

- What should the LPE Tool do if only the minimum spacing coefficient data are provided... Guess? Ignore? Use the value for minimum spacing?
- None of the above options are acceptable for deep sub-micron technologies . An accurate value must be known for all geometries
- Different widths of conductor and other geometries require different capacitance coefficients
 - E.g., A line over a line will result in a significantly different coefficient value compared to a line over a ground plane.

Interconnect Modeling

Introduction: Data Required for Deep Sub-Micron Designs (con't)

- Other typical configurations
 - 1/ Co-incident edges
 - 2/ Cross overs
 - 3/ Corners
 - 4/ Proximity effects

- EXACT can generate coefficients for ANY structure

Interconnect Modeling

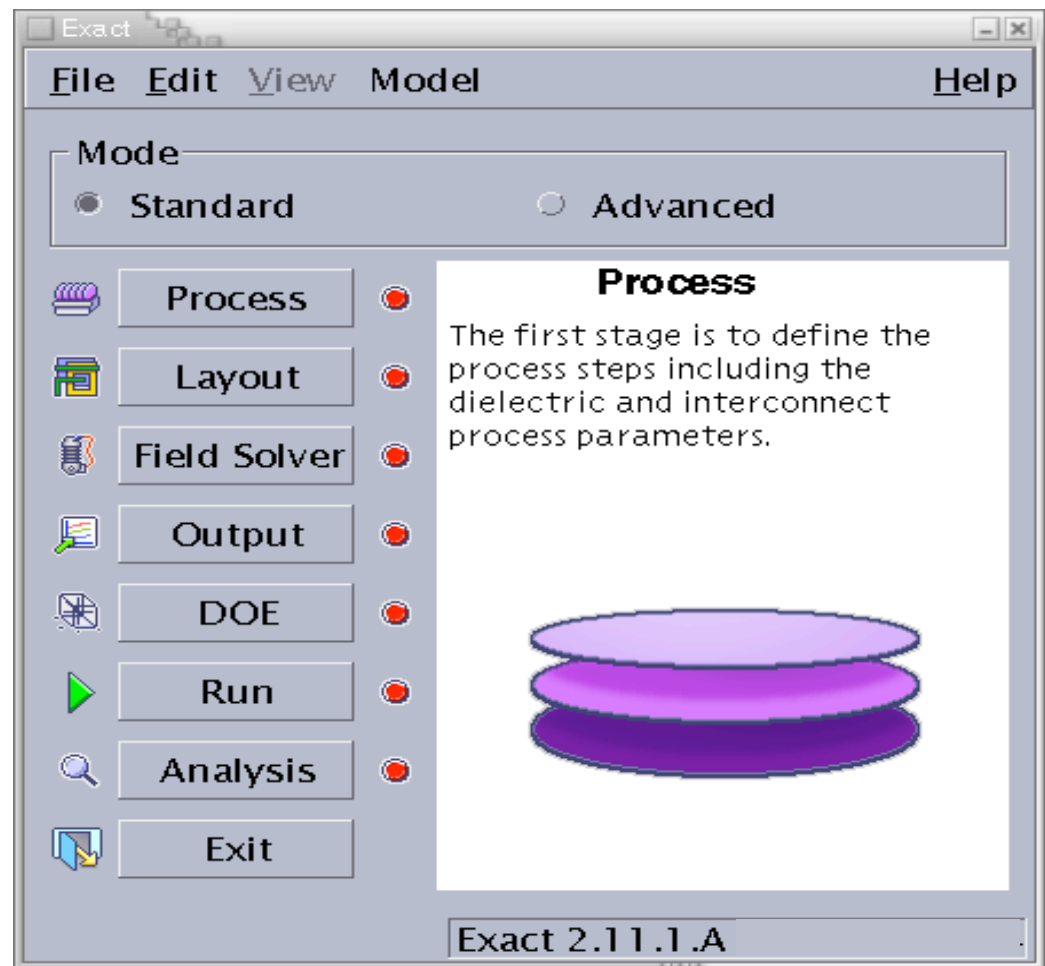
Workshop Summary

- Getting started
- Defining a process flow
 - (i) Simple processing using the Interactive Tool
 - (ii) Advanced process flow
- Defining and editing layout
- Test structures
- Defining the “Design of Experiments” (DOE)
- Executing the experiments
- Processing the data

Interconnect Modeling

EXACT GUI

- Type “EXACT” in a shell window to display this EXACT G.U.I.



Interconnect Modeling

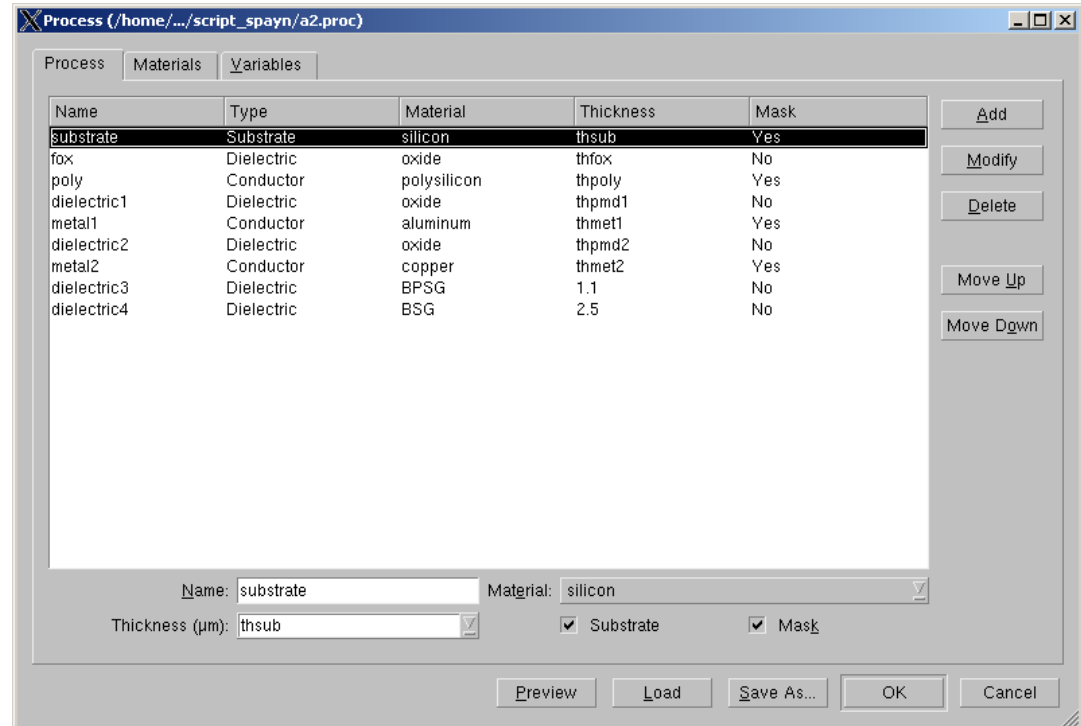
5 Stages of EXACT

- EXACT takes you through the 5 stages sequentially:
 - STAGE 1 Process Stage: Define the process
 - STAGE 2 Layout Stage: Define or load the test structure mask layouts
 - STAGE 3 Design of Experiments Stage: Select which experiments
 - STAGE 4 Run Stage: Run the experiments using the 3D process simulator and field solver
 - STAGE 5 Analysis Stage: Write or import a script to process all the data

Interconnect Modeling

Define the Process Flow: Standard Mode

- The Standard Mode option allows quick “interactive” creation of a simple process flow
- This creates simple “planar” structures
- Click “OK” when finished



Interconnect Modeling

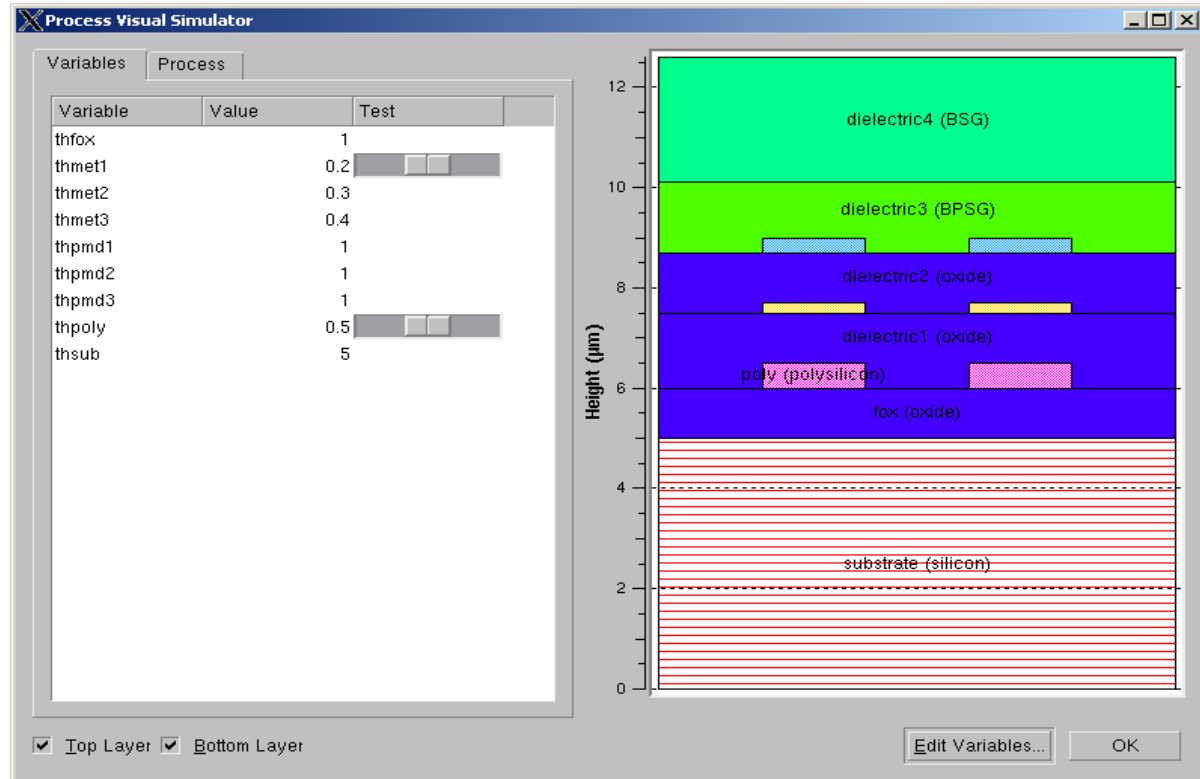
Define the Process Flow: Advanced Mode

- The Advanced Mode option allows the use of realistic photolithography, deposition or etching to create the test structures:
- In the Advanced mode users can:
 - i. create their own process flow
 - ii. edit a previous process flow from the interactive (from the Standard Mode) builder
 - iii. edit a CLEVER input deck
- We shall only deal with the Standard Mode option in this workshop

Interconnect Modeling

Process Preview with the Internal Viewer of EXACT

- Having entered the process via the Standard Mode, the process verification is made possible using the “process preview” button in the process GUI



Interconnect Modeling

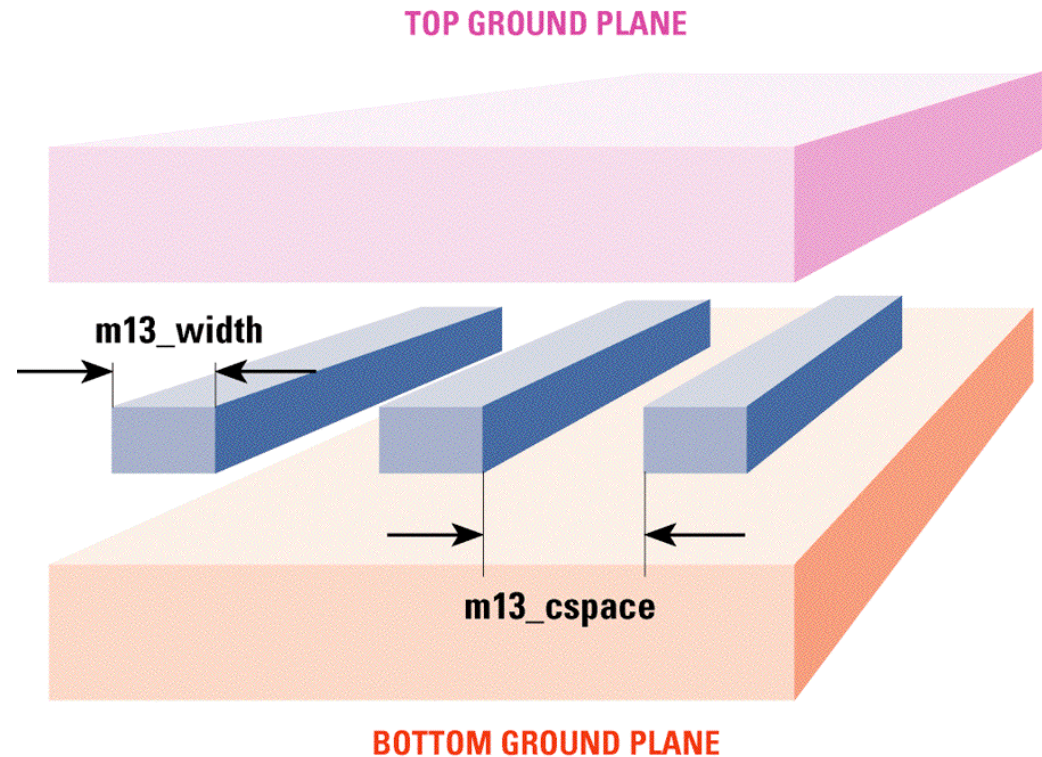
Layout Stage

- After having entered the process the test structure specific to which required capacitance coefficient are then loaded into EXACT
 - Standard generic test structures will be provided for various Extraction (LPE) Tools
 - Load test structures using the layout GUI
 - The layout GUI also allows user to create their own test structures using the “more options” mode of EXACT layout GUI

Interconnect Modeling

Example of a Layout Test Structure

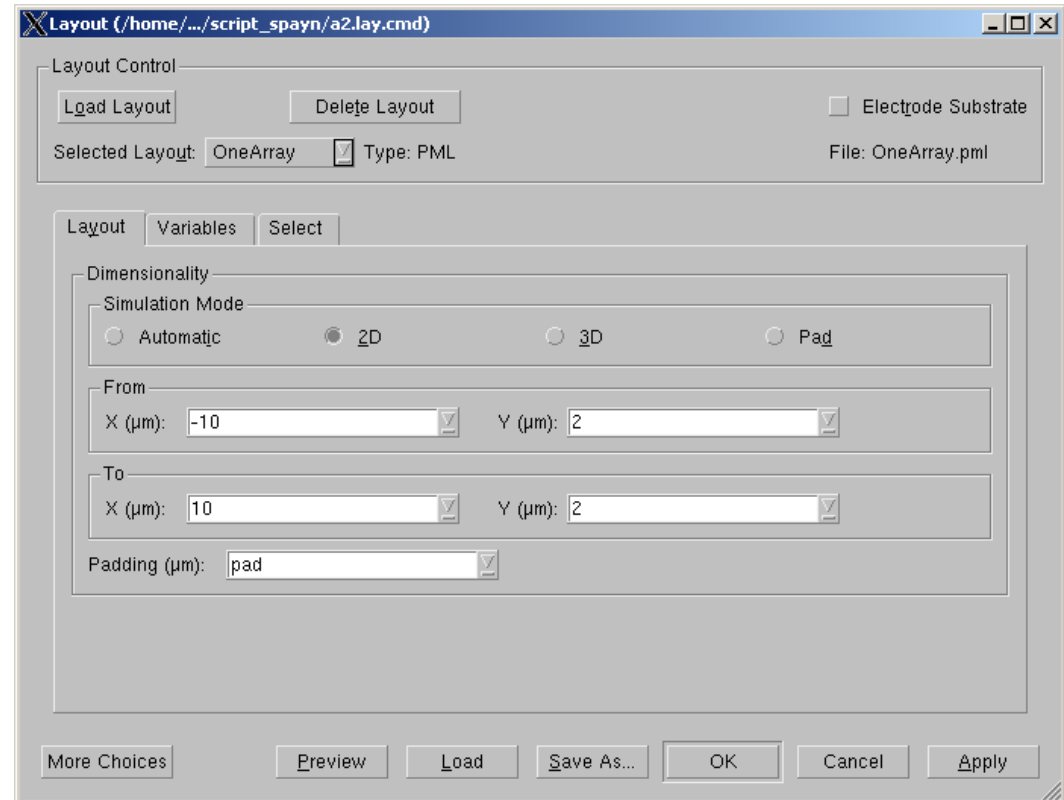
- An example of a layout test structure is shown here
- From the test structure capacitances such as near body capacitance (the capacitance between two wires of the same process layer) are easily obtained



Interconnect Modeling

Loading a Layout

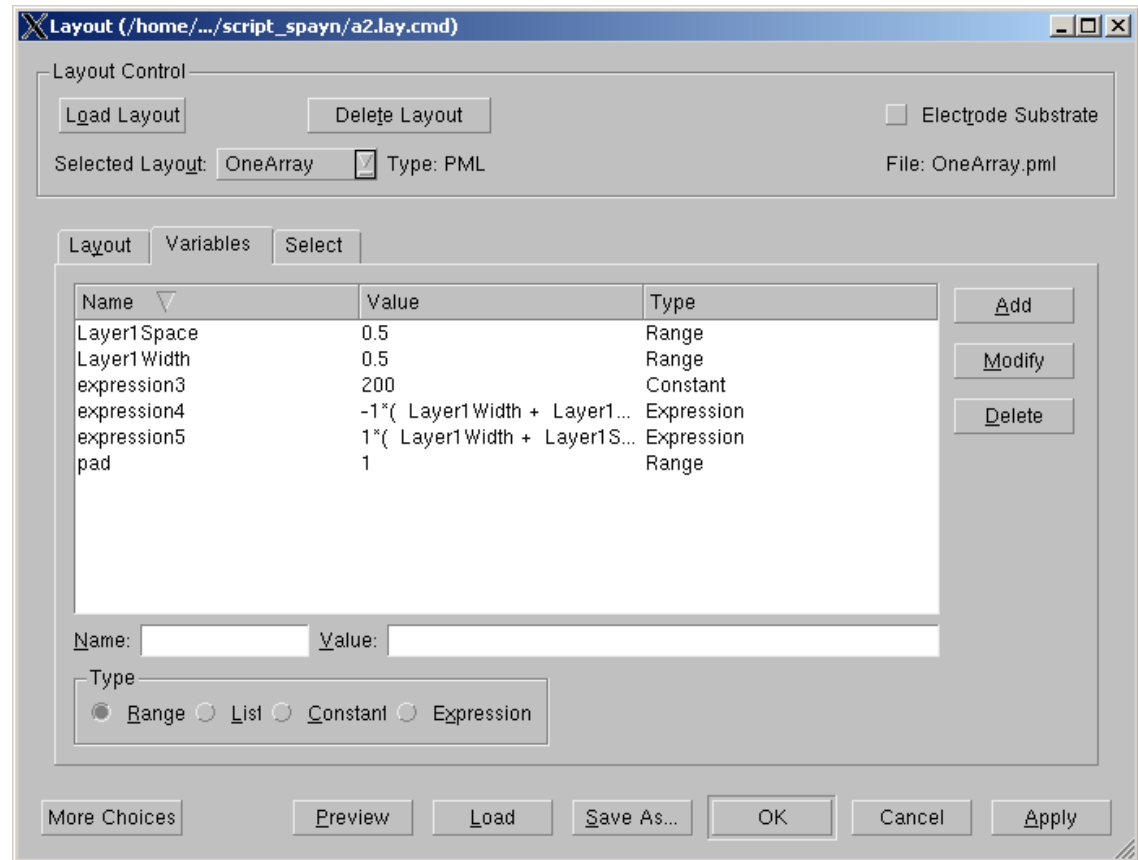
- Click “Layout...” to bring up the Layout Editor Window
- Click on load layout to load in a layout



Interconnect Modeling

Loading a Layout

- This figure shows the layout One Array that has been loaded into the layout GUI
- All of the layout definition is also shown



Interconnect Modeling

Creating a Layout: More Choices

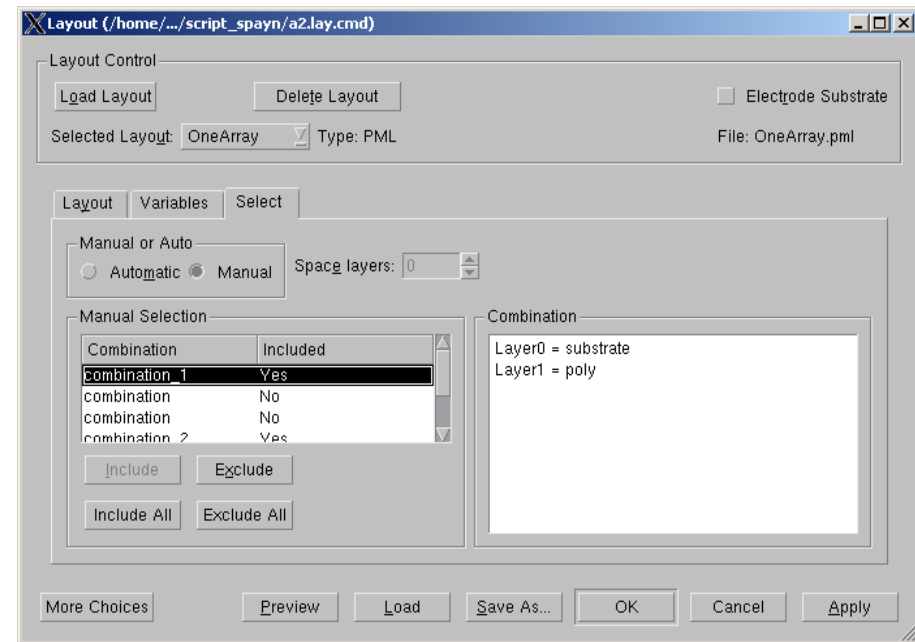
- By clicking on the “more choices” button in the layout GUI users have the ability to create a layout
- User defined layout: “layers” and “wires” button are added to allow you to define any kind of layout



Interconnect Modeling

Layout: Combination Selection

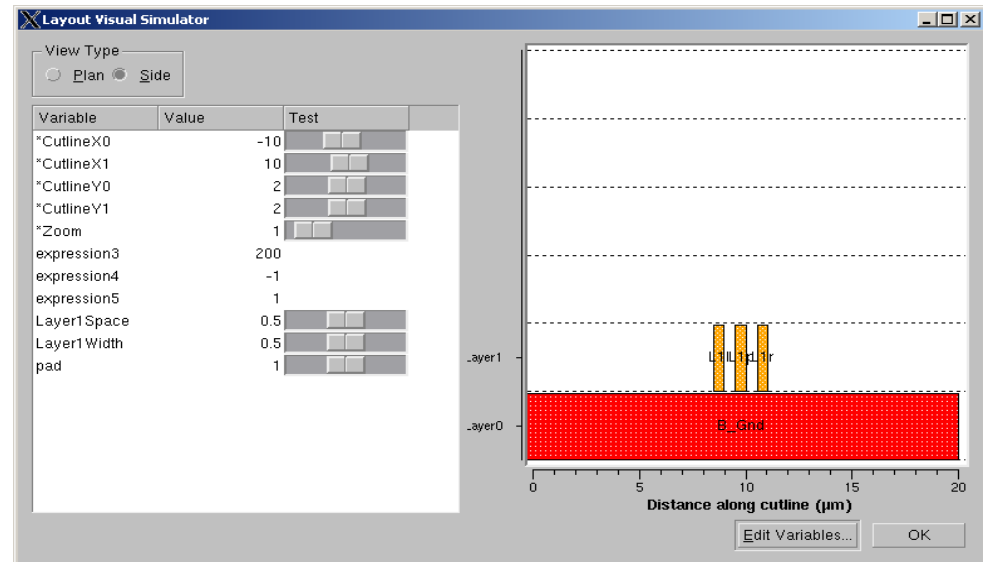
- Which process layers are assigned to which layout layers is performed via the combination selection in the layout GUI
- Select these by clicking on “Select”
- You may not be interested in all of them
- For example, you may not be interested in calculating the capacitance between Metal 4 and the substrate because they are very far apart
- You can select such combination individually, or use the automatic selection



Interconnect Modeling

Layout: Preview

- Any layout loaded into the layout GUI, or created in the GUI, can be viewed together with any dynamic properties it possesses
- Test structures in EXACT are defined using an interactive menu. Slide bars allow users to observe the effects of layout changes on the parameterized structure



Interconnect Modeling

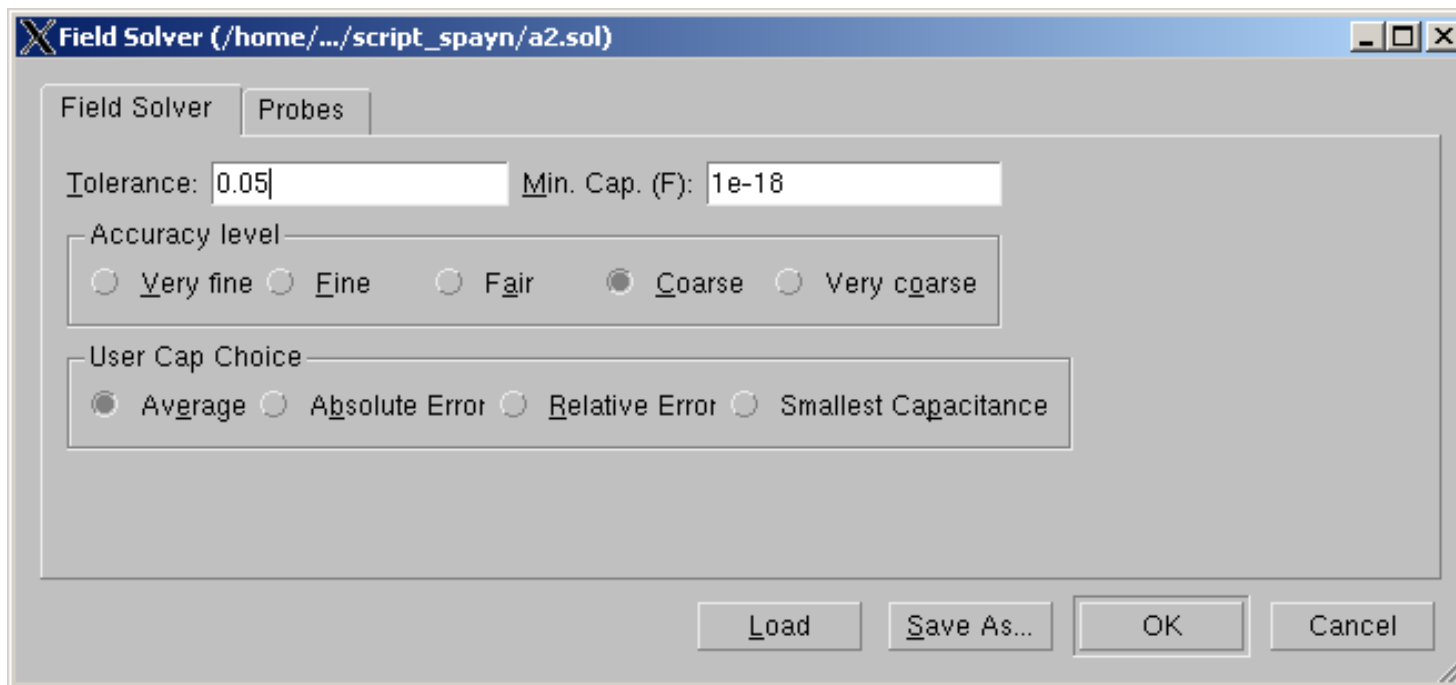
Layout: Preview

- To see each structure click on “preview”
- For plane view, click “plan”
- To see a cross-sectional view “side”
- This gives a cutline using the user definable co-ordinates in the 2D Cutline box
- To visualize the effect of varying the layout parameters, move sliders
- When in 2D or 3D mode use the sliders to vary the parameters

Interconnect Modeling

Field Solver

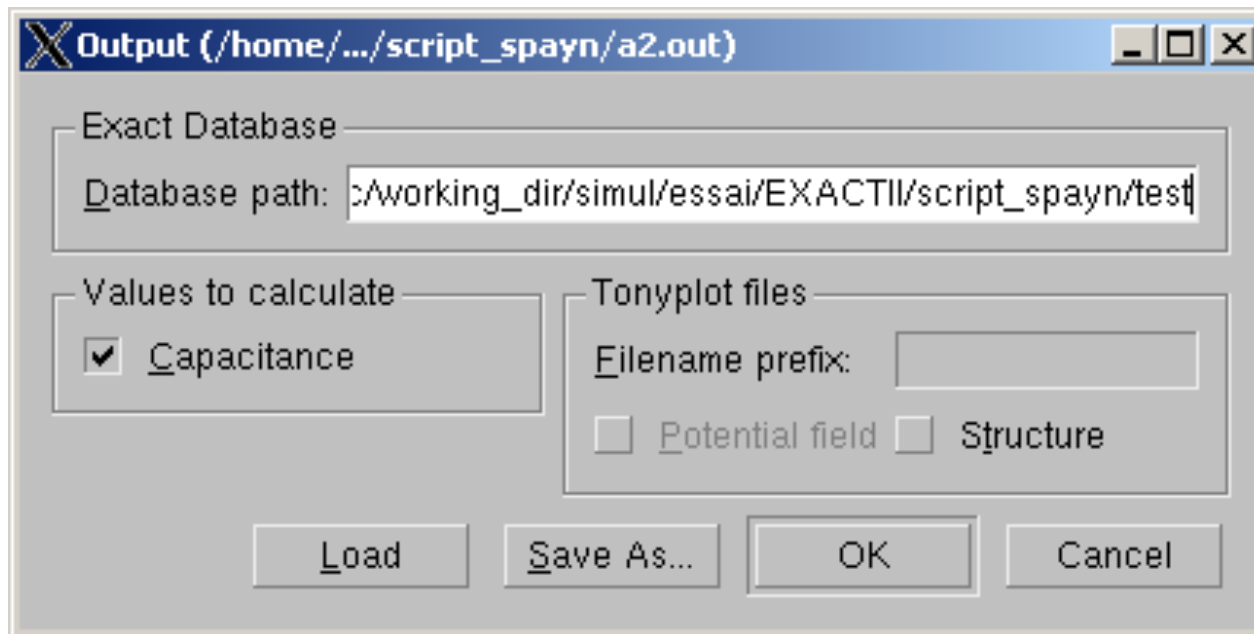
- Some control of the field solver attributes is given to the user. This figure shows the Field Solver GUI
- Use this window in EXACT to define the accuracy of the simulation using the “tolerance” and the “accuracy level” buttons



Interconnect Modeling

Output

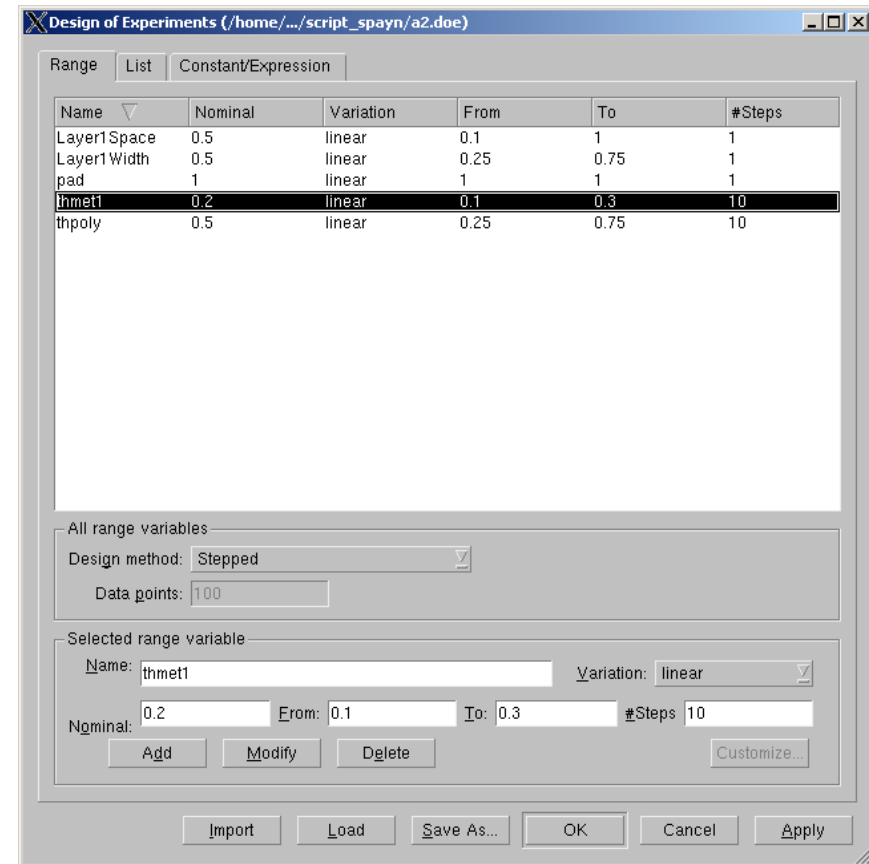
- Next we must define where the data that EXACT generates is to be stored, the output GUI, allows this to be done
- User defined database location where all the files will be stored
- Structure files can also be saved in order to be visualized using TonyPlot



Interconnect Modeling

DOE

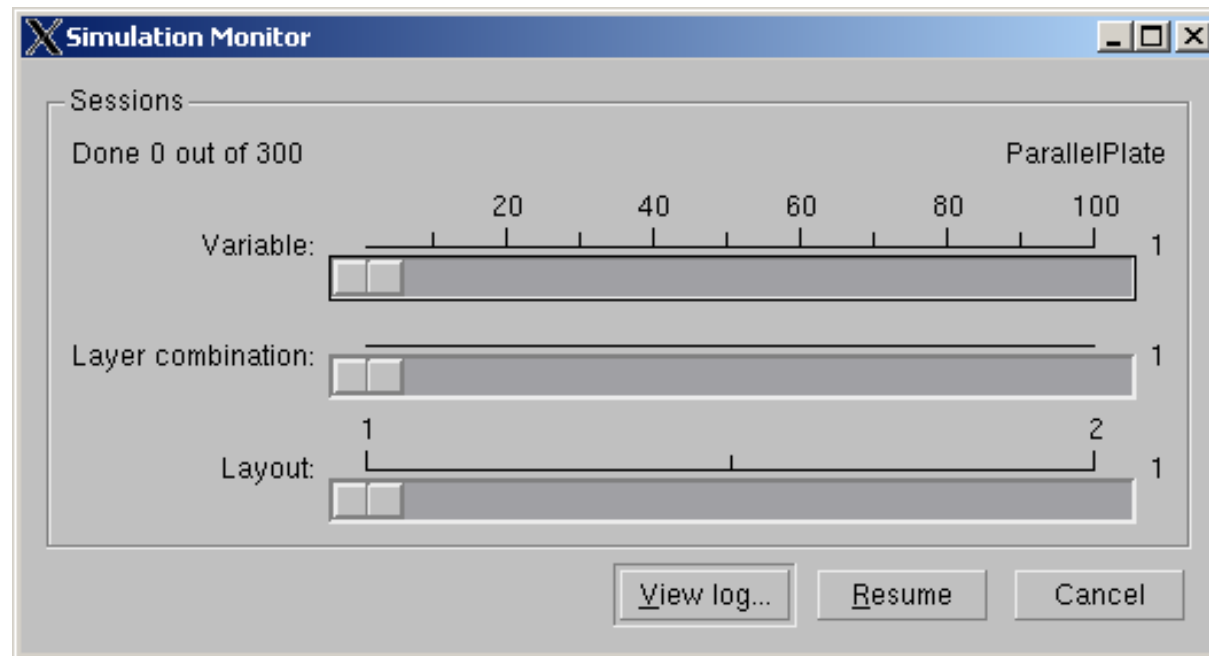
- The design of experiments stage is entered by clicking on the DOE button
- Click “DOE...” to bring up DOE window
- Use the DOE window to select the variable ranges and sample points
- Flexible design of experiment. (full factorial, stepped, ccc)
- Ability to change design parameters as well as process parameters



Interconnect Modeling

Running Simulations

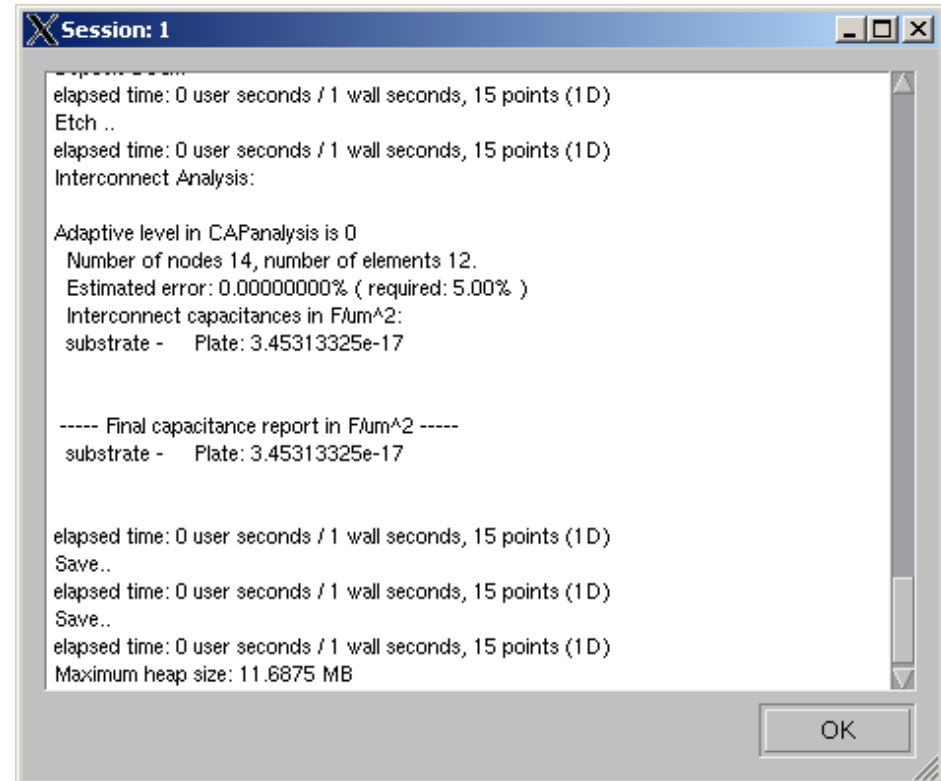
- After having finished setting up the simulation experiments, we can run them by clicking on the run button. The Run GUI open up is shown in this figure
- We can follow the running of the experiment
- At any stage in the execute window, click on view log shows the exact process flow being executed for that particular job (see figure on the following page)



Interconnect Modeling

Run

- At any moment in the run window, click the View Log... button for any of the experiments to visualize the exact process flow being executed for that particular job



```
Session: 1
elapsed time: 0 user seconds / 1 wall seconds, 15 points (1D)
Etch ..
elapsed time: 0 user seconds / 1 wall seconds, 15 points (1D)
Interconnect Analysis:

Adaptive level in CAPanalysis is 0
Number of nodes 14, number of elements 12.
Estimated error: 0.00000000% ( required: 5.00% )
Interconnect capacitances in F/um^2:
substrate - Plate: 3.45313325e-17

----- Final capacitance report in F/um^2 -----
substrate - Plate: 3.45313325e-17

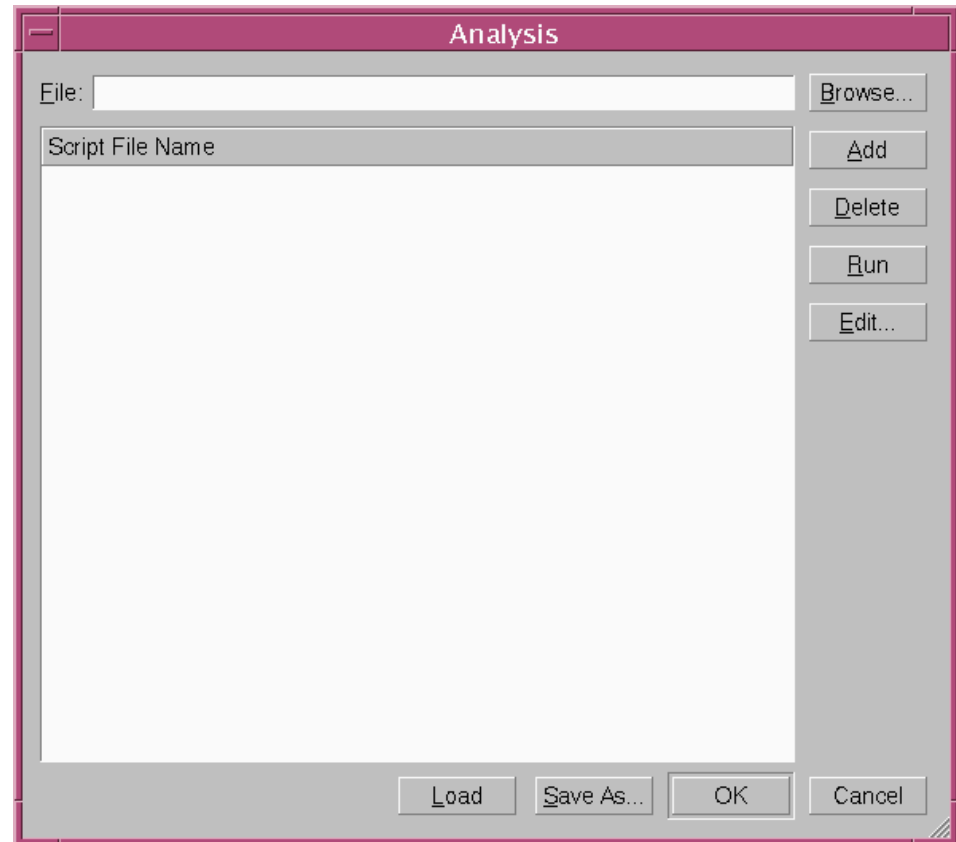
elapsed time: 0 user seconds / 1 wall seconds, 15 points (1D)
Save..
elapsed time: 0 user seconds / 1 wall seconds, 15 points (1D)
Save..
elapsed time: 0 user seconds / 1 wall seconds, 15 points (1D)
Maximum heap size: 11.6875 MB
```

OK

Interconnect Modeling

Analysis Stage

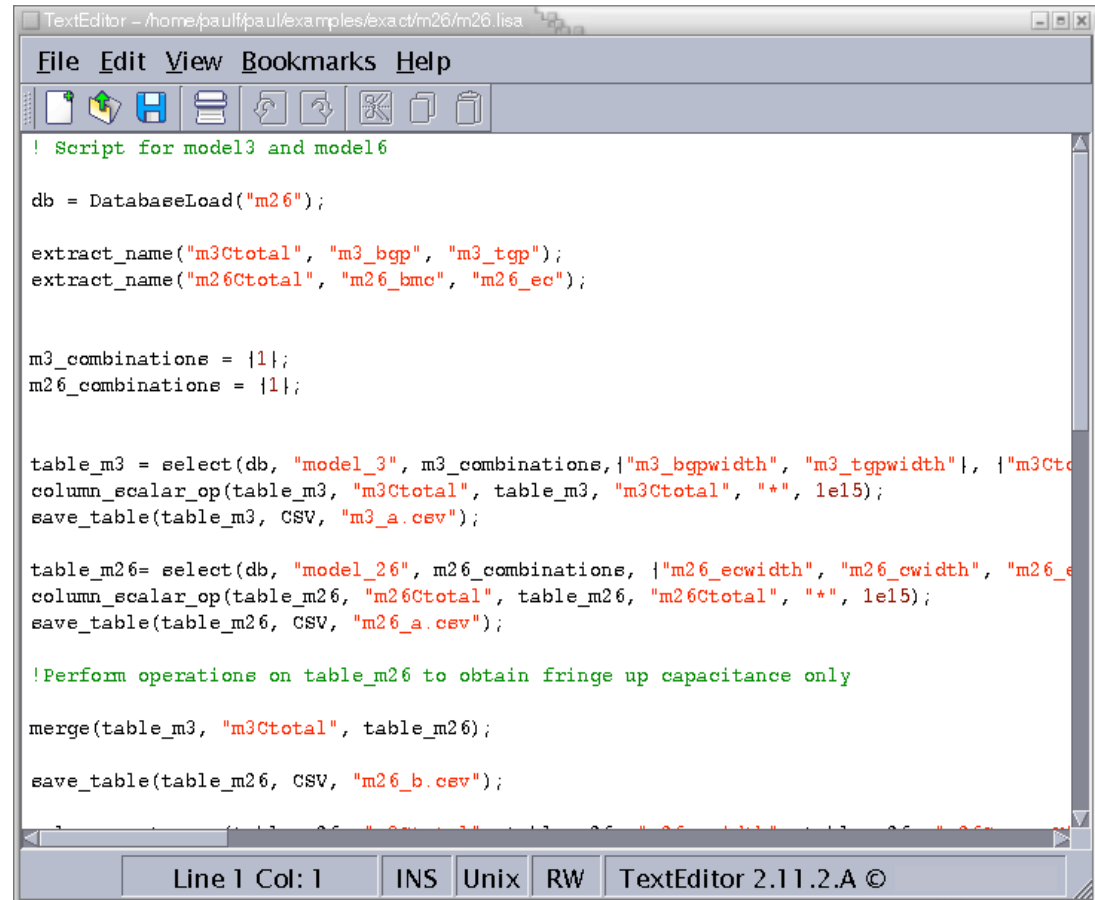
- Once the experiments have been simulated, click on the analysis window
- We provide scripts to plot all the data (CSV and TonyPlot format)
- The user must now write scripts to format data to LPE tools specific format. We provide templates for Diva™, XCalibre™, and HIPEX
- Direct link to SPAYN



Interconnect Modeling

Analysis: Script

- Load a script file (written in LISA)
- In this example a script has been loaded into the Analysis Stage



```
TextEditor - /home/paul/paul/examples/exact/m26/m26.lisa
File Edit View Bookmarks Help
! Script for model3 and model6

db = DatabaseLoad("m26");

extract_name("m3Ctotal", "m3_bgp", "m3_tgp");
extract_name("m26Ctotal", "m26_bmc", "m26_ec");

m3_combinations = {1};
m26_combinations = {1};

table_m3 = select(db, "model_3", m3_combinations, {"m3_bgpwidth", "m3_tgpwidth"}, {"m3Ctotal",
column_scalar_op(table_m3, "m3Ctotal", table_m3, "m3Ctotal", "+", 1e15);
save_table(table_m3, CSV, "m3_a.csv");

table_m26= select(db, "model_26", m26_combinations, {"m26_ecwidth", "m26_cwidth", "m26_e
column_scalar_op(table_m26, "m26Ctotal", table_m26, "m26Ctotal", "+", 1e15);
save_table(table_m26, CSV, "m26_a.csv");

!Perform operations on table_m26 to obtain fringe up capacitance only

merge(table_m3, "m3Ctotal", table_m26);

save_table(table_m26, CSV, "m26_b.csv");

Line 1 Col: 1   INS  Unix  RW  TextEditor 2.11.2.A ©
```

Interconnect Modeling

Analysis: Script Output

- Mentor Graphics xCalibre™/Calibre xRC™ rule file generated by EXACT using the associated script file

```
CAPACITANCE INTRINSIC FRINGE metal2
[
    PROPERTY C
    max_caldistance = 5
    max_distance = 3
    C= 0.0
    if (distance() > 0.0) {
        C = 0.01001*(1.0 - exp(-1.65*(distance()+0.075)))*length()
    }
    if (distance() <= 0.0) {
        C = 0.0304042* length()
    }
]

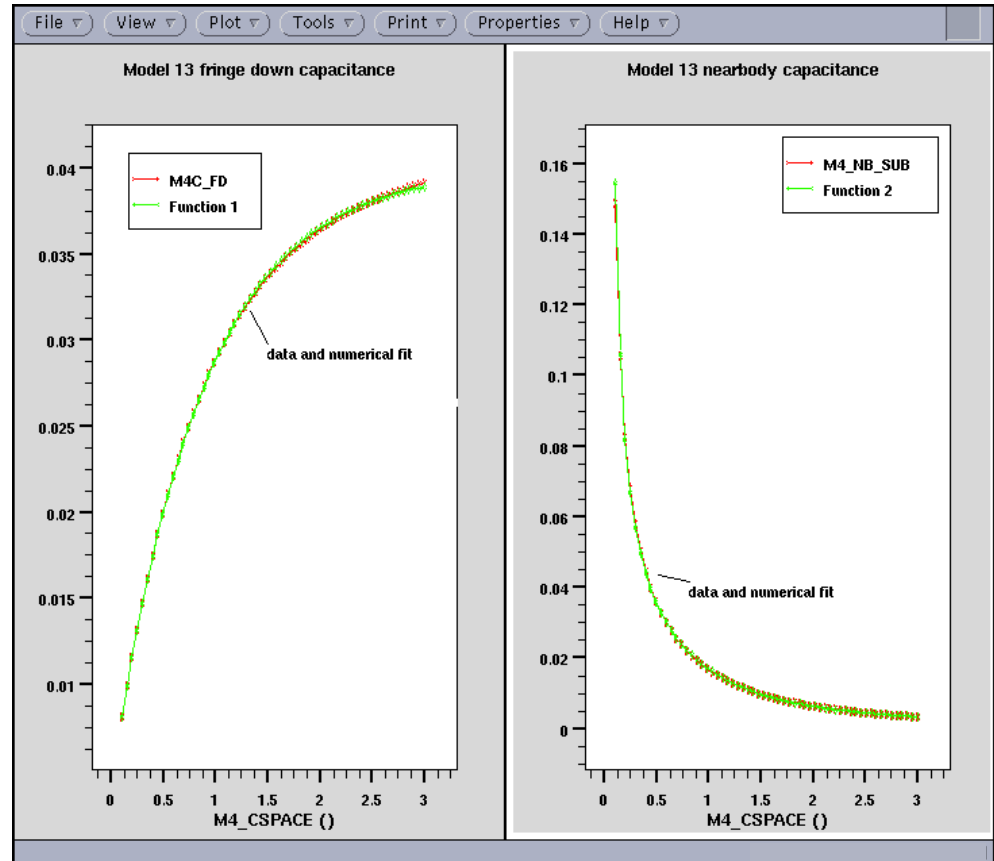
CAPACITANCE NEARBODY poly1

[
    PROPERTY C
    max_width = 3
    max_distance = 3
    C=0.932762*length()*pow(0.1,0.0536348)*1.0*(exp((-distance()*1.60124)-2.96352)
        + (0.00677904/pow(distance(),1.3288)))
]
]
```

Interconnect Modeling

Filed Solver Results

- Field solver results and fitted equation for the structure on the left



Interconnect Modeling

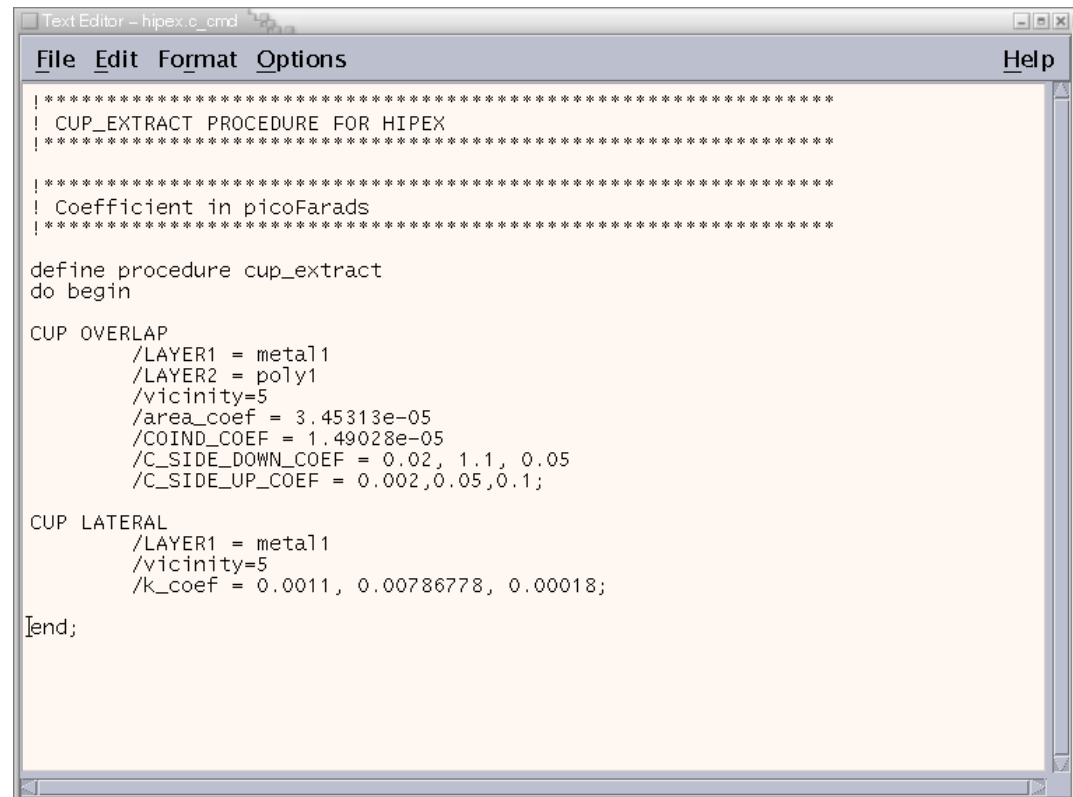
Automatic Models

- Exact can automate the generation of parameters for use in Hipex
- Define a process (in either Standard or Advanced mode)
- Select the Model->Hipex menu
- Exact will load a set of pre-defined layouts that it needs, and run a series of simulations and perform equation fitting to generate the Hipex parameters, all automatically
- You can override the default for the variables used
- Exact saves a LISA file for HIPEX, and saves all of its own project files

Interconnect Modeling

Model HIPEX Output

- Extract from a HIPEXscript generated with 'Model Hipex'



```
Text Editor - hipex.c_cmd
File Edit Format Options Help
|*****
| CUP_EXTRACT PROCEDURE FOR HIPEX
|*****
|*****
| Coefficient in picoFarads
|*****

define procedure cup_extract
do begin
CUP OVERLAP
  /LAYER1 = metal1
  /LAYER2 = poly1
  /vicinity=5
  /area_coef = 3.45313e-05
  /COIND_COEF = 1.49028e-05
  /C_SIDE_DOWN_COEF = 0.02, 1.1, 0.05
  /C_SIDE_UP_COEF = 0.002,0.05,0.1;

CUP LATERAL
  /LAYER1 = metal1
  /vicinity=5
  /k_coef = 0.0011, 0.00786778, 0.00018;

end;
```

Interconnect Modeling

Summary

- Today we have shown you how simple it is to use “EXACT”
 - To create or use existing test structures using a real process flow
 - Either realistic or simple 3D processing can be used
 - Set up and run a design of experiments using a 3D field solver
 - Process the data for LPE tools
- EXACT (will) increases the accuracy of full chip parasitic extraction
- EXACT can be used in conjunction with ANY full chip extraction tool