

Light-emitting organic field-effect transistor using an organic heterostructure within the transistor channel

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(Received 31 March 2006; accepted 12 October 2006; published online 28 November 2006)

The authors have realized a light-emitting organic field-effect transistor. Excitons are generated at the interface between a *n*-type and a *p*-type organic semiconductor heterostructure inside the transistor channel. The dimensions and the position of the *p-n* heterostructure are defined by photolithography. The *p-n* heterostructure is at a distance of several microns from the metal electrodes. Therefore, the exciton and photon quenching in this device is reduced. Numerical simulations fit well with the experimental data and show that the light-emitting zone can move within the transistor channel. © 2006 American Institute of Physics. [DOI: 10.1063/1.2392937]

Organic semiconductors have been incorporated in a number of devices, such as organic thin-film transistors (OTFTs) and circuits, organic solar cells, and organic light-emitting diodes (OLEDs). Display applications are particularly important drivers for the further development of this organic technology.

Light-emitting organic field-effect transistors (LEOFETs) may become interesting structures in this field, as they combine the optical output of an OLED and the gate control of an OTFT in a single device. Moreover, LEOFETs are interesting devices in order to study the optoelectronic properties of organic semiconductors.

Since the first demonstration of a LEOFET in 2003,¹ LEOFETs have been fabricated using polymers,^{2,3} small molecules,^{4,5} and a heterostructure of a *p*-type and a *n*-type organic semiconductor.⁶ Recently, results were published on LEOFETs based on an ambipolar polymeric semiconductor.⁷ A recent overview of light-emitting organic transistors can be found in literature.⁸

In this letter, a structure is proposed in which excitons are generated at the interface of a *n*-type and a *p*-type semiconductor. In contrast to previously published heterostructure LEOFETs, in our device the location and the dimensions of the overlap between the semiconductors are defined by photolithography.

The advantage of our structure, as compared to traditional (heterostructure) LEOFETs, is twofold. First, the recombination zone is easily confined within the transistor channel at a distance of several microns from the metal source and drain contacts. Our device is therefore expected to have a reduced exciton and photon quenching at the contacts, resulting in higher optical intensity.

Like in other types of LEOFETs, the recombination region in our device shifts within the transistor channel by changing the biasing conditions.⁷ Although one could argue that the exact position of the recombination region can be

controlled by appropriate biasing, and a patterned heterostructure is therefore not necessary, our device does lead to a second advantage as compared to nonpatterned heterostructure LEOFETs. The magnitude of the movement of the light-emitting region in the channel, which we define as the distance the recombination region moves per volt that is applied at the gate (expressed in $\mu\text{m}/\text{V}$), is largely determined by the ratio of the electron and hole mobilities in the device.⁷ When these parameters differ significantly, as is often the case, the exact position of the light-emitting zone is very sensitive to the applied gate bias. In a nonpatterned heterostructure LEOFET, an increase of the gate bias of a few volts can therefore cause the light-emitting zone to shift across the complete transistor channel. If this is the case, it is very hard to confine the light-emitting region in the middle of the channel by choosing appropriate biasing conditions; the excitons are almost certainly quenched, either by the source or by the drain electrode. It will be demonstrated that our device, on the other hand, is not sensitive to the ratio of the electron and hole mobilities. Indeed, even when the electron and hole mobilities differ significantly, and the position of the recombination region is very sensitive to the biasing conditions, the light-emitting zone will never reach the source electrode due to the fact that the heterojunction pins the recombination zone in the middle of the channel over a large gate bias range.

In order to obtain the proposed behavior, devices were processed on a highly doped *n++* Si wafer, acting both as the substrate and the gate electrode. The gate dielectric is a layer of 100 nm thermally grown SiO₂. Source and drain electrodes consist of a layer of 20 nm Au, patterned by optical lithography and lift-off. On top of this structure, a 5 μm thick layer of a positive photoresist is patterned by optical lithography. This photoresist profile in fact creates a shadow mask that is integrated with the substrate.⁹

1,4-bis(octyloxy)-2,5-bis[(*E*)-4-(*E*)-styrylstyryl]benzene (O-octyl-OPV5), an oligo(phenylene vinylene) derivative [highest occupied molecular orbital (HOMO)=5.49 eV, lowest unoccupied molecular orbital (LUMO)=2.9 eV, as measured by cyclic voltammetry¹⁰], was used as the *p*-type semiconductor.¹¹ After a cleaning step, 50 nm of O-octyl-OPV5 is evaporated in ultrahigh vacuum, while the substrate is tilted over a +45° angle relative to the molecular flux.

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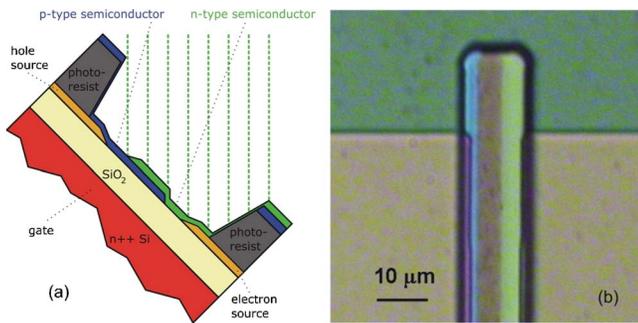


FIG. 1. (Color online) (a) Schematic illustration of the *n*-type semiconductor deposition and (b) microphotograph of the finished device.

Because of the tilted deposition through the integrated shadow mask, the *p*-type semiconductor is covering one metal electrode completely, as well as part of the channel. The other metal electrode is in the shadow of the integrated shadow mask during the evaporation, hence no *p*-type material is deposited there.

N,N'-ditritylperylene-3,4,9,10-tetracarboxylic diimide (PTCDI-C₁₃H₂₇), a perylene derivative (HOMO = 5.4 eV, LUMO = 3.4 eV), was used as the *n*-type semiconductor.^{6,12} 50 nm of PTCDI-C₁₃H₂₇ is evaporated in ultrahigh vacuum, while keeping the substrate over a -45° angle relative to the flux, as schematically illustrated in Fig. 1(a). As can be verified from the micrograph in Fig. 1(b), this method can be used to realize a device in which a *p-n* heterostructure is patterned within the transistor channel. This zone is relatively far (in the order of a few micrometers) from the metal electrodes.

By applying a bias to the gate, source, and drain electrodes, charge carriers can be injected from the source and drain contacts into the organic semiconducting films. In fact, the traditional nomenclature of source and drain is ambiguous in this type of device, since both electrodes do inject carriers in the organic materials, and neither of them actually drains carriers. Therefore, from now on, we will refer to the

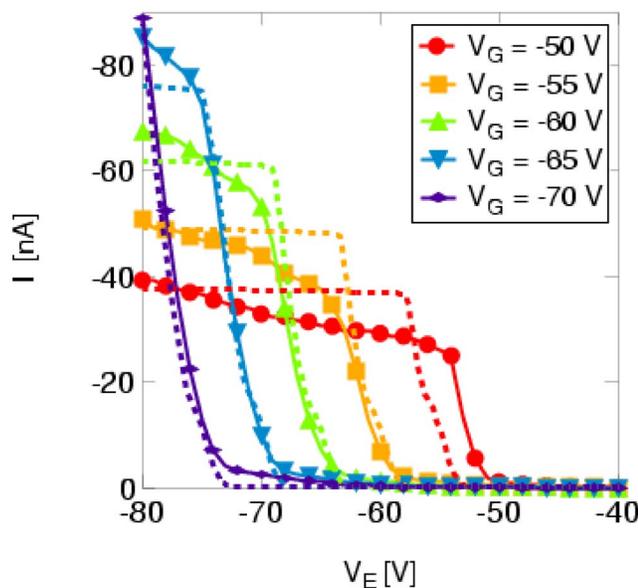


FIG. 2. (Color online) Electrical characteristics of the device, experimentally measured (solid curves) and simulated (dashed curves). $W/L=20$ in both cases.

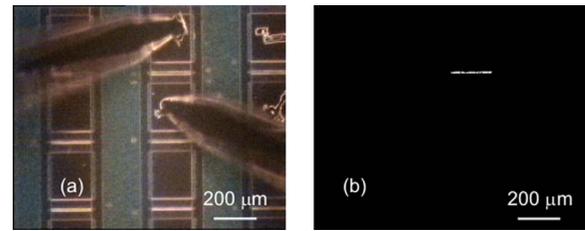


FIG. 3. (Color online) Optical microscope image of (a) the measurement setup and (b) the optical output upon bias ($W/L=200/10$).

electrode that injects holes in the *p*-type semiconductor as the hole source. The hole source is also the electrode that is held at ground potential ($V_H=0$). The electron source, at potential V_E , is defined as the electrode that is connected to the *n*-type semiconductor.

The experimentally measured electrical characteristics of the device are shown as the solid lines in Fig. 2. The device was measured in an inert N₂ atmosphere immediately after the *n*-type semiconductor deposition using an Agilent 4156C parameter analyzer. The electrical characteristics can be qualitatively explained as follows: for a fixed negative gate voltage V_G , holes are injected from the hole source into the *p*-type material, and a hole accumulation layer is formed. Since the HOMOs of both organic semiconductors are almost equal to each other, holes encounter a negligible barrier at the *p-n* junction; thus, the hole accumulation layer extends over the complete transistor channel. In a first operation regime, for electron source voltages $|V_E| < |V_G - V_{T,n}|$ (in which $V_{T,n}$ is the threshold voltage of the *n*-type material), there is only a very low current. Indeed, the hole mobility in PTCDI-C₁₃H₂₇ is low, and in this regime, there are no electrons available yet which the holes can recombine with.

As soon as $|V_E| \geq |V_G - V_{T,n}|$, the device enters a second operation regime. Electrons are injected from the electron source into the *n*-type material, forming an electron accumulation layer. The electron and hole accumulation layers meet somewhere in the channel, and every hole transported from the hole source through the *p*-type material is expected to recombine with an electron that is carried from the electron source through the *n*-type semiconductor. The current through the device increases quadratically, as can be expected for any *n*-type transistor of which V_G and V_D are constant, while V_S decreases. This is equivalent to a *n*-type transistor with a constant V_S , while V_G and V_D increase simultaneously and at the same rate, which indeed leads to a quadratic current-voltage characteristic.

At a certain electron source voltage V_E , the electron current in the *n*-type material becomes equal to the possible hole current in the *p*-type material. From this voltage on, the LE-OFET operates in a third regime. Indeed, in contrast to previously published LE-OFETs,^{6,7} increasing $|V_E|$ beyond this voltage leads to a saturation of the current. This is explained by the fact that the current in this kind of device is limited by the smallest of the electron and the hole currents. In this third operation regime, the *p*-type OTFT is in saturation, and its saturated current limits the overall current through the device. A further increase in $|V_E|$ merely pushes the *p*-type OTFT further in saturation and does not significantly increase its saturation current.

When the biasing conditions are such that the potential at some point in the channel equals the gate potential, the

TABLE I. Summary of the material parameters used in the two-dimensional device simulator.

	O-octyl-OPV5	PTCDI-C ₁₃ H ₂₇
LUMO (eV)	2.9	3.4
HOMO (eV)	5.4	5.4
μ_e (cm ² /V s)	1×10^{-8}	2.5×10^{-2}
μ_h (cm ² /V s)	3.5×10^{-4}	1×10^{-8}
V_T (V)	-15	3

accumulated charge at that place is zero, and consequently, the electron and hole accumulation layers meet at this point. Excitonic recombination of electrons and holes occurs at this place. It was indeed experimentally confirmed that the device emits light upon the radiative decay of the excitons. Figures 3(a) and 3(b) illustrate the measurement setup and the resulting optical output, respectively. The intensity of the light clearly increases with the electron and hole currents, caused by increasing $|V_G|$. The emitted light could be observed by the naked eye.

The device was simulated using the Silvaco ATLAS two-dimensional device simulator. The material parameters used in the simulations are summarized in Table I. The geometry used in the simulations is shown as dashed lines in Fig. 4. The simulated characteristics nicely fit with the experimentally observed electrical data, as shown in Fig. 2. The quantitative differences between the measured data and the simulated behavior can be explained by the fact that the model we used for simulating the device does not incorporate second order effects, such as a gate bias dependent mobility, contact effects, etc.

It is assumed that the light emission zone moves within the transistor channel, exactly as has been previously described by Zaumseil *et al.*⁷ Due to the small dimensions of our device and the fact that our measurement setup is not equipped with a microscope with sufficiently high magnification, we have been unsuccessful in demonstrating this experimentally. However, this assumption is supported by numerical simulations.

Figure 4 clearly illustrates that the recombination region moves from right to left (i.e., from the *n* region to the *p* region) by increasing $|V_E|$ while keeping V_G at a fixed negative value. At $V_E \approx V_G - V_{T,n}$, weak recombination occurs at the gate dielectric-organic interface in the *n*-type material, very close to the electron injecting electrode. For these biasing conditions, injected electrons are readily available; the holes are carried from the hole source electrode through the *p*-type material and encounter a negligibly low barrier at the *p*-*n* interface. At more negative values of V_E , the position where the channel potential equals V_G moves to the left. As a consequence, holes and electrons meet at a position that moves towards the hole source electrode. At a sufficiently negative V_E , the recombination zone is located at the far edge of the *n*-type material. Electrons face a relatively high injection barrier at the interface with the *p*-type material. Hence, the recombination zone does not move further. Instead, simu-

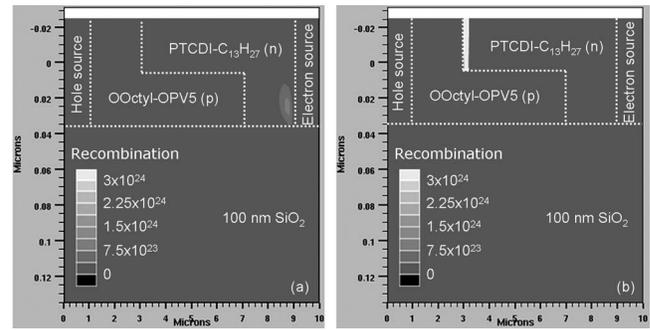


FIG. 4. Numerical simulations indicate that the recombination zone moves within the transistor channel. (a) $V_E \approx V_G - V_{T,n}$ and (b) $V_E \ll V_G - V_{T,n}$.

lations show that the recombination zone increases in height when $|V_E|$ is further increased.

In conclusion, we have realized a light-emitting organic field-effect transistor based on a heterostructure of a *n*- and a *p*-type organic semiconductor. The heterostructure is confined inside the transistor channel by photolithography. The location and the dimensions of the overlapping zone between the two semiconductors can be controlled. This allows for positioning the electron-hole recombination region several microns away from the metal hole source and electron source electrodes, leading to reduced exciton and photon quenching. Upon appropriate biasing, we have observed the emission of a relatively bright light. Numerical simulations show that the actual recombination region shifts within the transistor channel by changing the biasing conditions, confirming previously published experimental results.

This work is partially supported by the EU-funded Research Projects OLAS (Contract No. 015034) and BIOPOLTRONIC (Contract No. 509233). The authors gratefully acknowledge Sofie Fourier (Hasselt University) for performing the cyclic voltammetry experiments on O-octyl-OPV5.

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