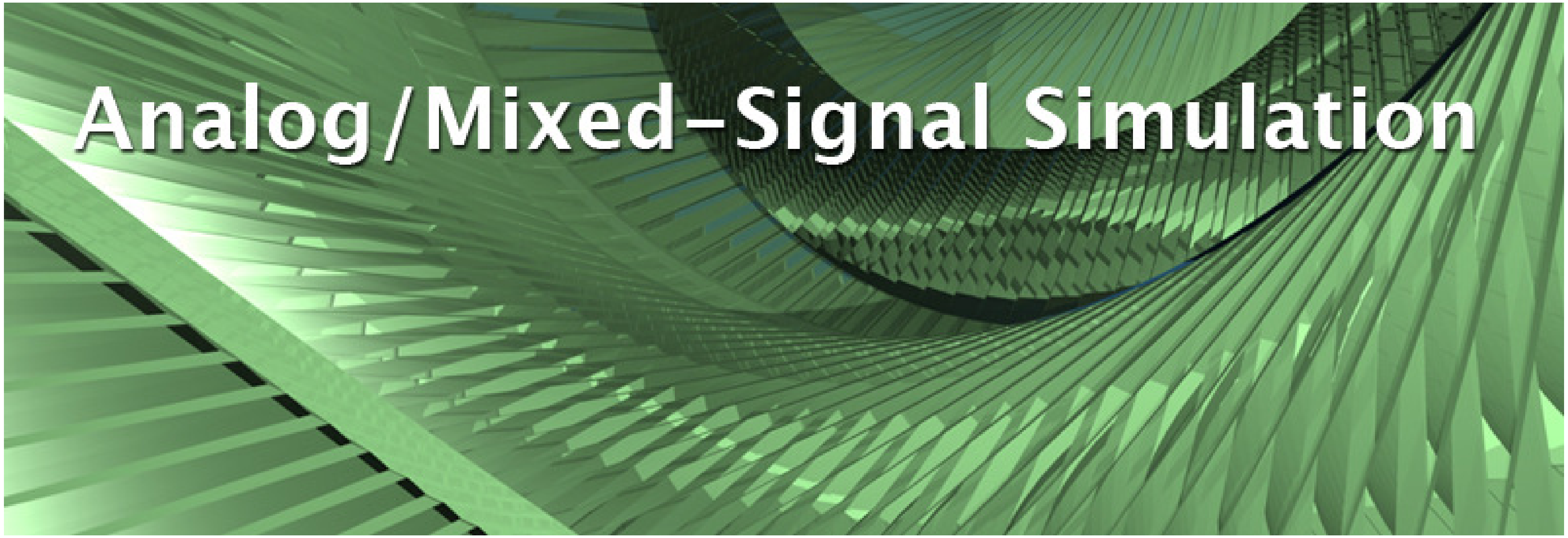
BSIMCMG model parameter extraction



September, 2011

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Overview

•BSIMCMG parameter optimization: environment

•BSIMCMG model

•UTMOST IV BSIMCMG parameter optimization sequence

•Basic flow of MOS model parameter optimization

BSIMCMG parameter optimization: environment

•UTMOST IV:

1.7.11.R: The hybrid optimizer should be set as GA+LM. The number of simulations is four.

•SmartSpice:

4.1.53.C is used for BSIMCMG v.105.3 (ModelLib v.1.8.5.)

•SmartView:

2.25.40.R

•Multi-core machine which becomes available commonly is recommended for the execution of UTMOST IV optimization.

•The execution time for three devices was 17 min. on 2GHz 2 core machine.

BSIMCMG model -1

•No BSIMCMG model equation is documented including UC Berkeley PhD dissertations.

http://www.eecs.berkeley.edu/Pubs/TechRpts/2008/EECS-2008-20.html

http://www.eecs.berkeley.edu/Pubs/TechRpts/2011/EECS-2011-69.html

•Silvaco ModelLib user's manual (Sep. 14. 2011) description is for BSIMCMG 105.0. BSIMCMG 105.3 (the latest) update which is used in this UTMOST IV project is documented in the release note.

•SmartSpice 4.1.53.C is required for the version 105.3.

•BSIMCMG users have to figure out the model parameter effects initially from the parameter names, and next from using UTMOST IV rubberband.

BSIMCMG model -2

•Length scaling of VSAT and VSAT1 parameters such as AVSAT, BVSAT, AVSAT1 and BVSAT1 are found to have no effect.

•Current fit errors are quite satisfactory: 2 to 3 % for all IdVd characteristics.

•UTMOST IV model parameter ranges are defined for current targets of the uds data set. The modification might become necessary for other devices.

UTMOST IV BSIMCMG optimization sequence-1

•UTMOST IV optimization sequence follows the basic flow of MOS model parameter optimization which is attached in this document.

•The model parameters of EOT is used, not TOXP.

•The TFIN and HFIN parameters which are respectively for the FIN thickness and the height work together as the channel width. The former is the instance parameter. The usual instance parameter of width isn't used.

•The HFIN together with the XL(channel length modification) parameters are necessary for the capacitance fitting. They adjust the gate area to meet the gate capacitance. And they should be fixed for the succeeding steps.

UTMOST IV BSIMCMG optimization sequence-2

•The NBODY (channel doping concentration) and the PHIG (work function of gate) parameters are optimized for the threshold voltage.

•The DVT0(SCE coefficient) and DVT1(SCE exponent coefficient) should be reserved for the threshold voltage dependency on the drain bias.

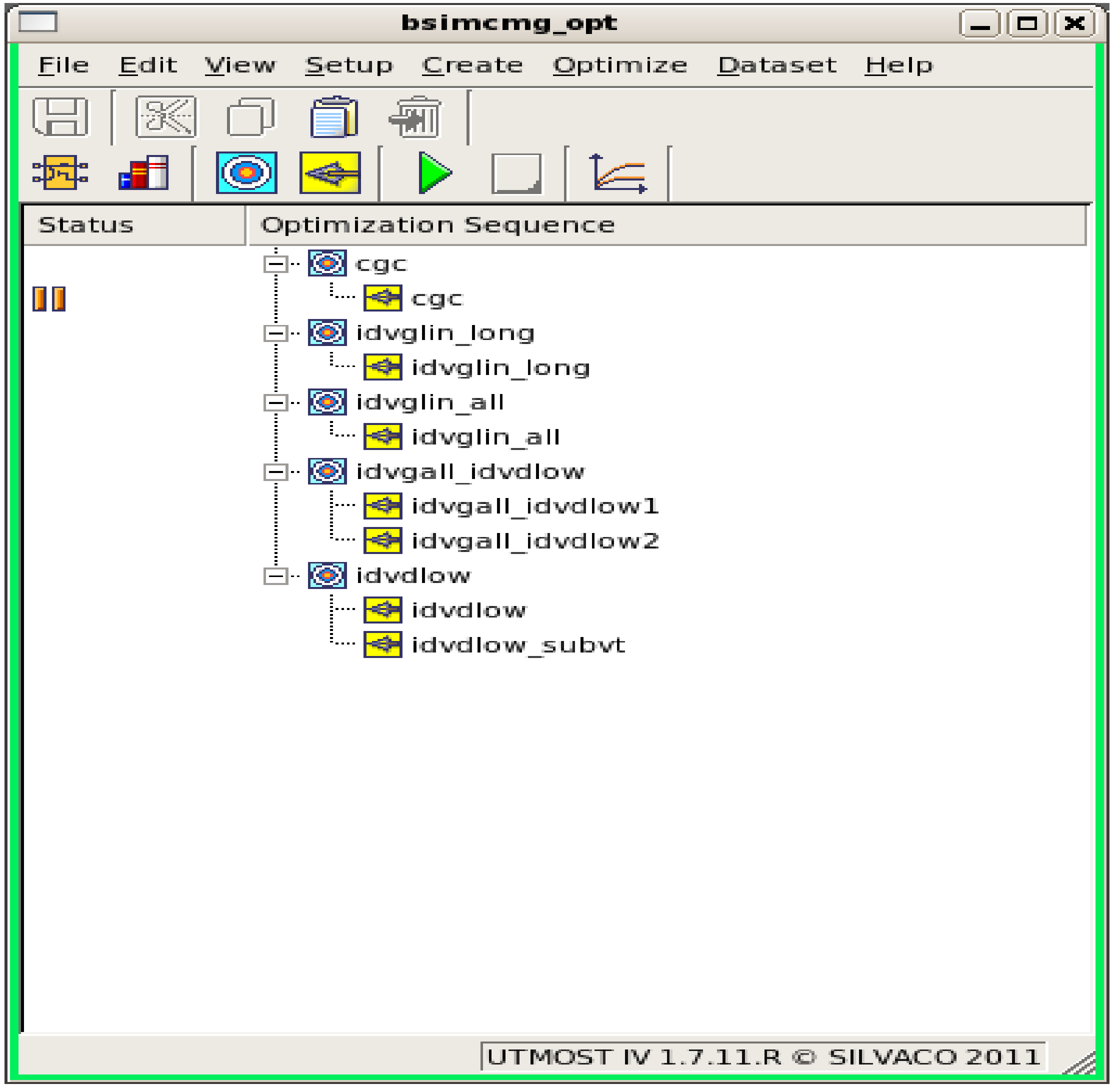
•One of the steps in the optimization sequence uses Genetic Algorithm optimizer alone. The intention is to get the proper initial values for the saturation model parameters. The simulation curves would be evenly close to the targets. The use of Levenberg Marquardt as the hybrid with G.A. went into the one sided result, which suggested the solution was the local minimum.

UTMOST IV BSIMCMG optimization sequence-3

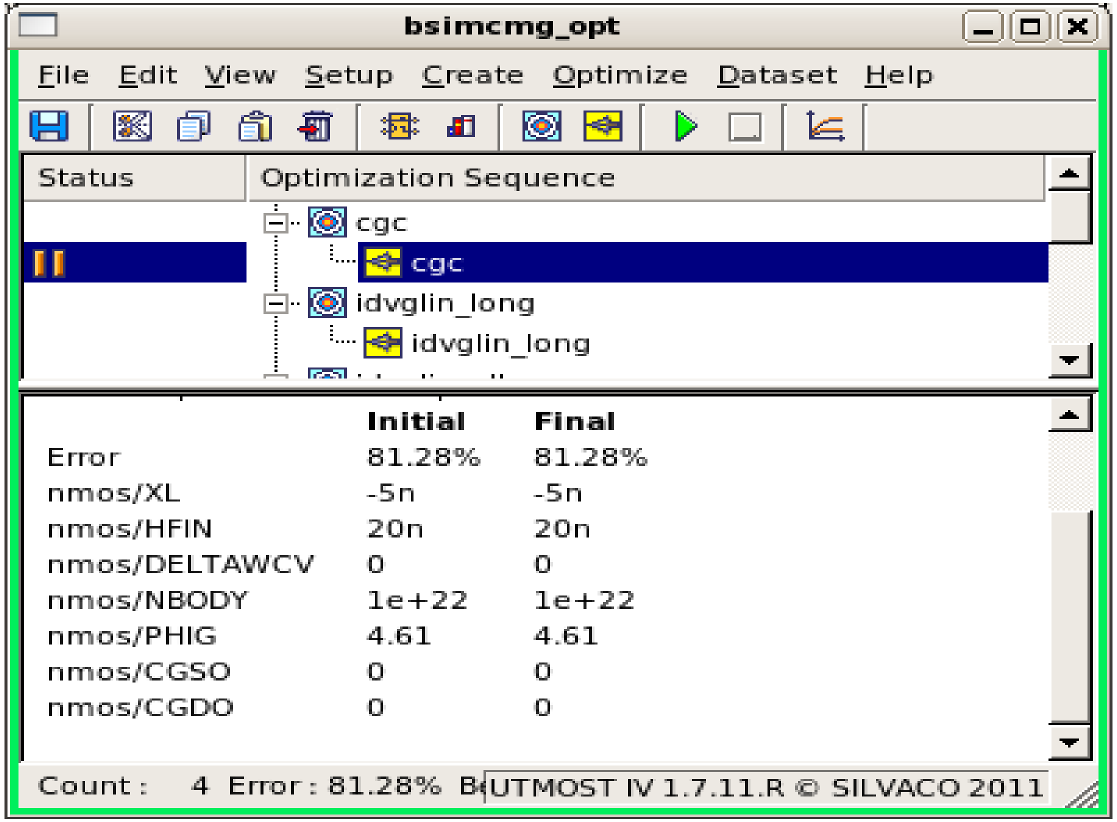
•The sub-threshold swing is controlled by the CIT (parameter for interface trap).

•BCMCMG 105.3 capacitance model appears to need the slight improvement for the flexible gate bias dependency.

UTMOST IV BSIMCMG optimization sequence



UTMOST IV BSIMCMG optimization sequence- cgc



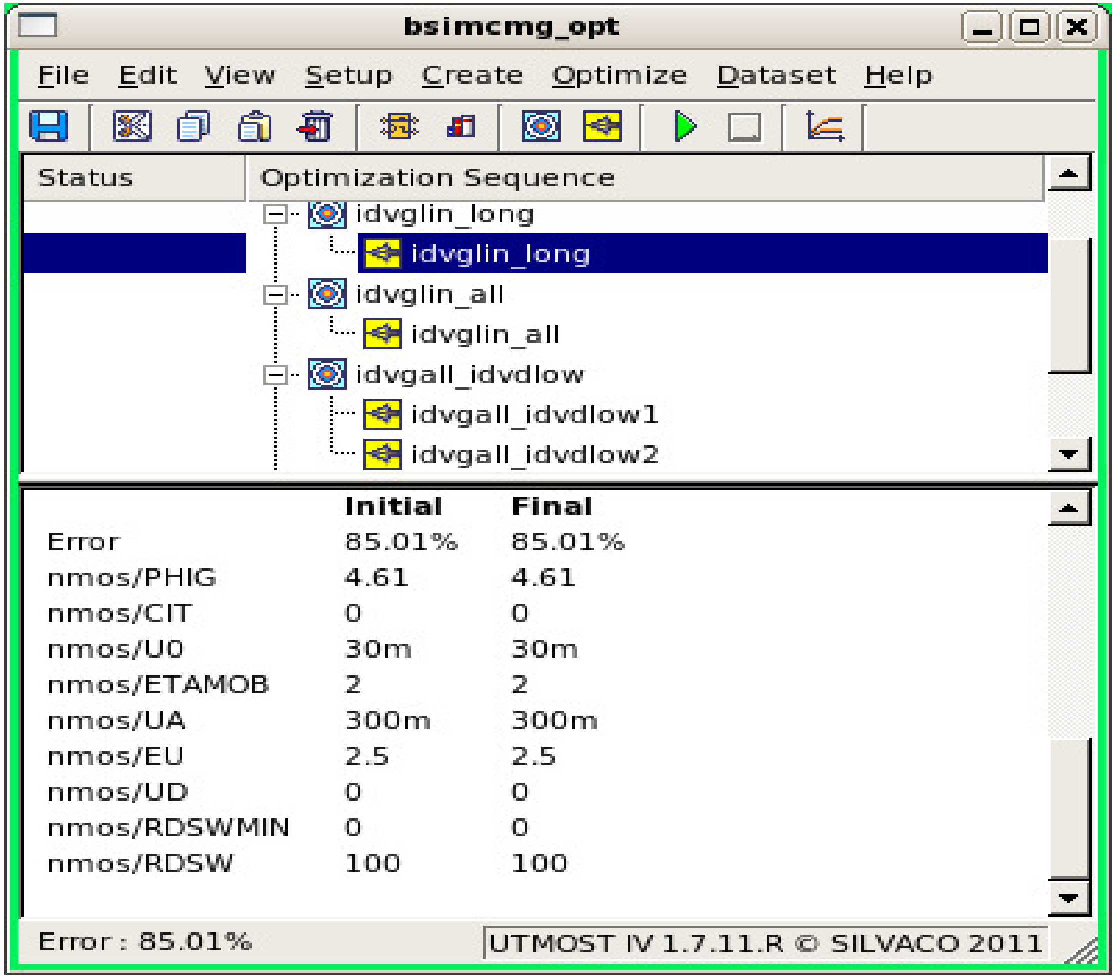
- Target:

  gate capacitance

- Optimizer:

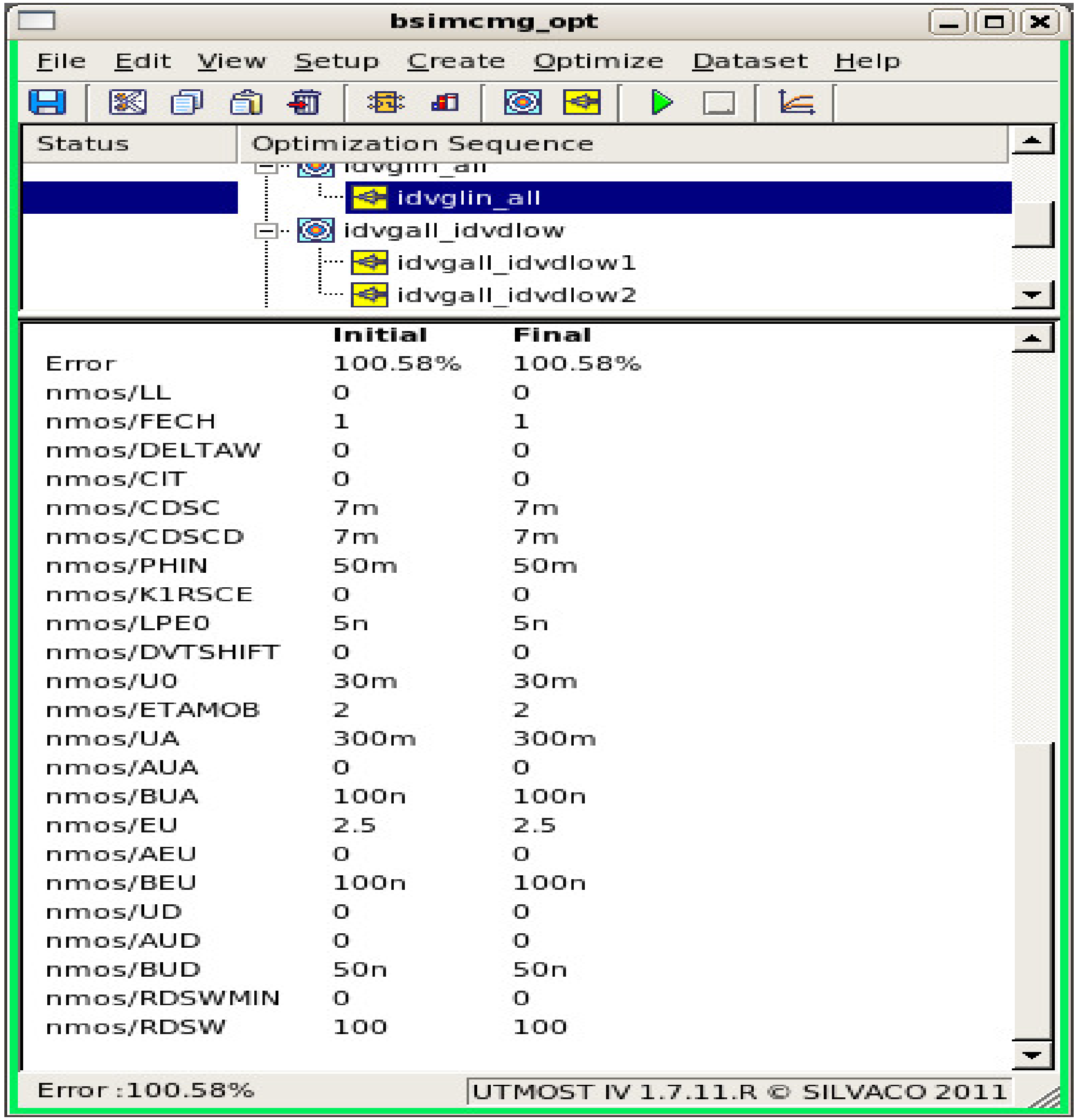
  Hybrid (GA + LM)

UTMOST IV BSIMCMG optimization sequence- idvglin



- Target:
  long channel
  idvg @linear vds
- Optimizer:
  Hybrid (GA + LM)

UTMOST IV BSIMCMG optimization sequence- idvglin_all



- Target:
  scaled length
  idvg @linear vds
- Optimizer:
  Hybrid (GA + LM)

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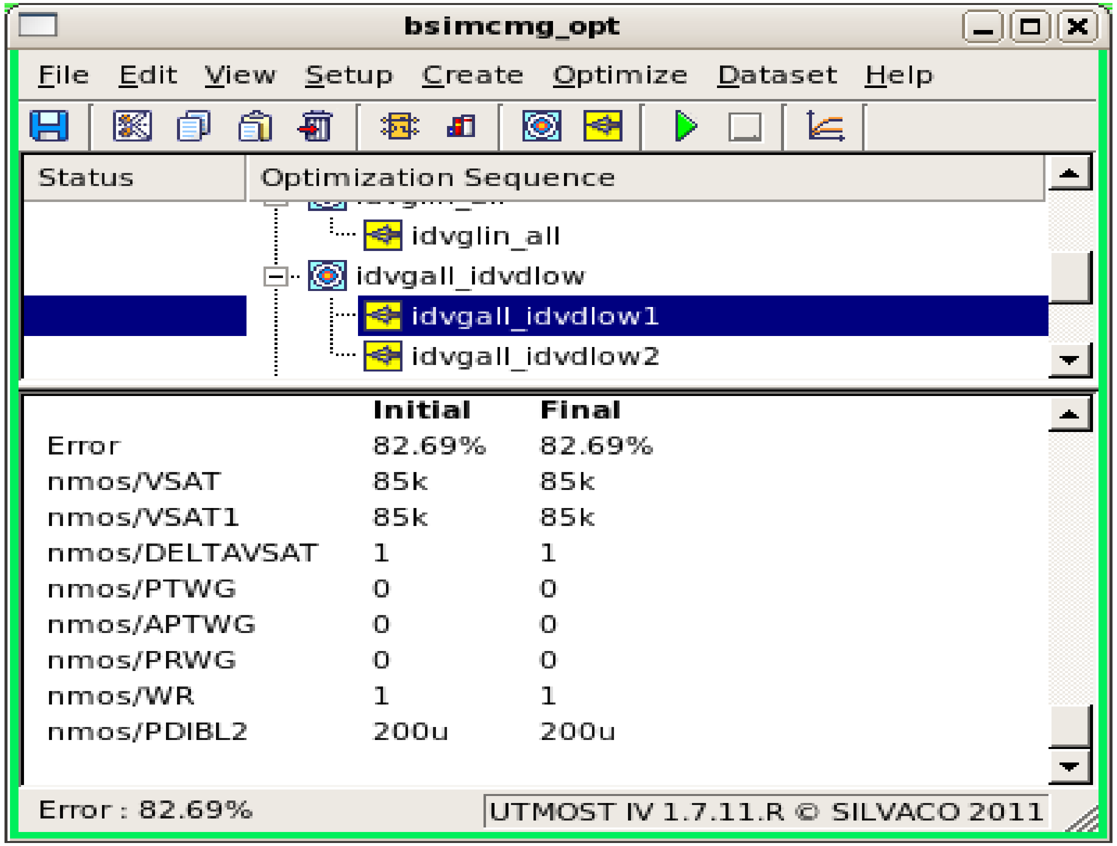
UTMOST IV BSIMCMG optimization sequence- idvgall_idvd



- Target:

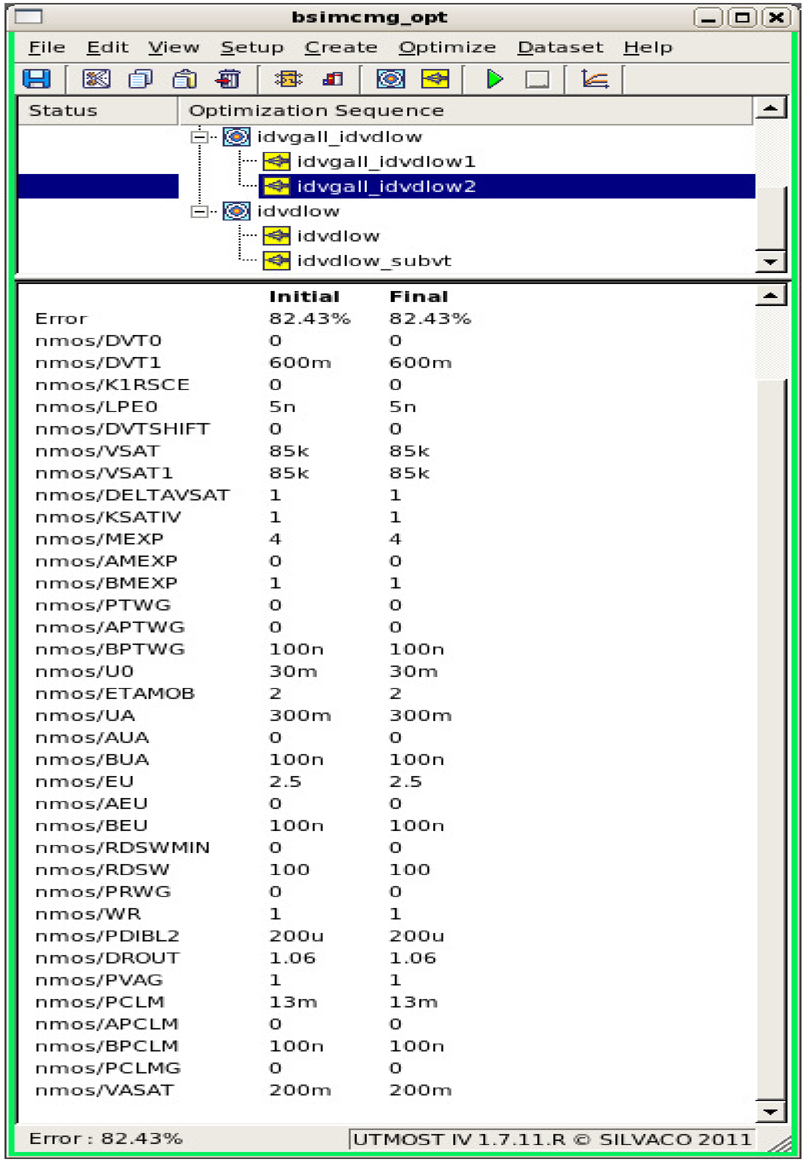
  scaled length

  idvg @linear/saturation vds & idvd

- Optimizer:

  Genetic algorithm

UTMOST IV BSIMCMG optimization sequence- idvgall_idvd



	Initial	Final
Error	82.43%	82.43%
nmos/DVT0	0	0
nmos/DVT1	600m	600m
nmos/K1RSCE	0	0
nmos/LPE0	5n	5n
nmos/DVTSHIFT	0	0
nmos/VSAT	85k	85k
nmos/VSAT1	85k	85k
nmos/DELTAVSAT	1	1
nmos/KSATIV	1	1
nmos/MEXP	4	4
nmos/AMEXP	0	0
nmos/BMEXP	1	1
nmos/PTWG	0	0
nmos/APTWG	0	0
nmos/BPTWG	100n	100n
nmos/U0	30m	30m
nmos/ETAMOB	2	2
nmos/UA	300m	300m
nmos/AUA	0	0
nmos/BUA	100n	100n
nmos/EU	2.5	2.5
nmos/AEU	0	0
nmos/BEU	100n	100n
nmos/RDSWMIN	0	0
nmos/RDSW	100	100
nmos/PRWG	0	0
nmos/WR	1	1
nmos/PDIBL2	200u	200u
nmos/DROUT	1.06	1.06
nmos/PVAG	1	1
nmos/PCLM	13m	13m
nmos/APCLM	0	0
nmos/BPCLM	100n	100n
nmos/PCLMG	0	0
nmos/VASAT	200m	200m

- Target:

  scaled length

  idvg @linear/saturation vds

  & idvd
- Optimizer:

  Levenberg Marquardt

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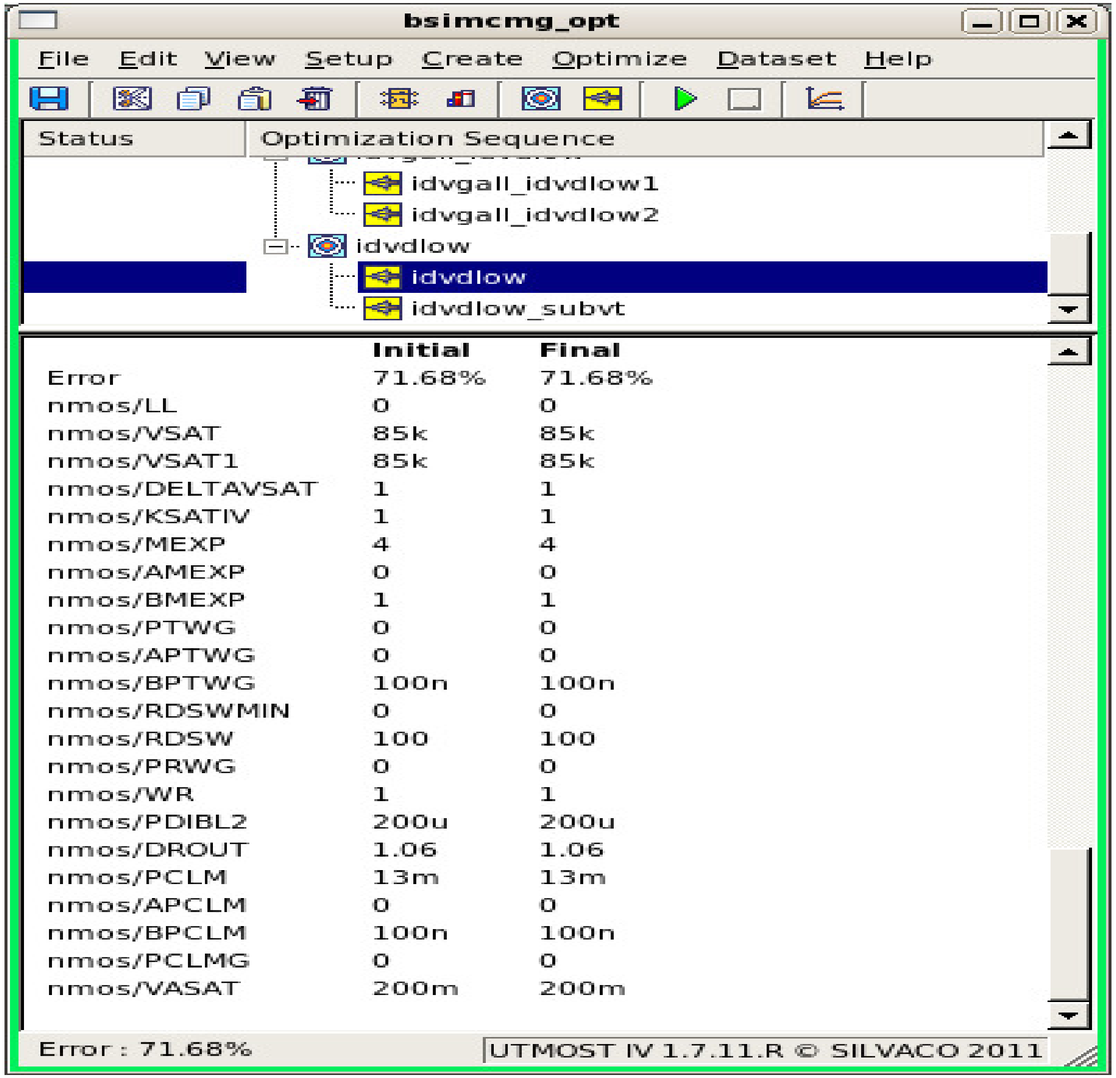
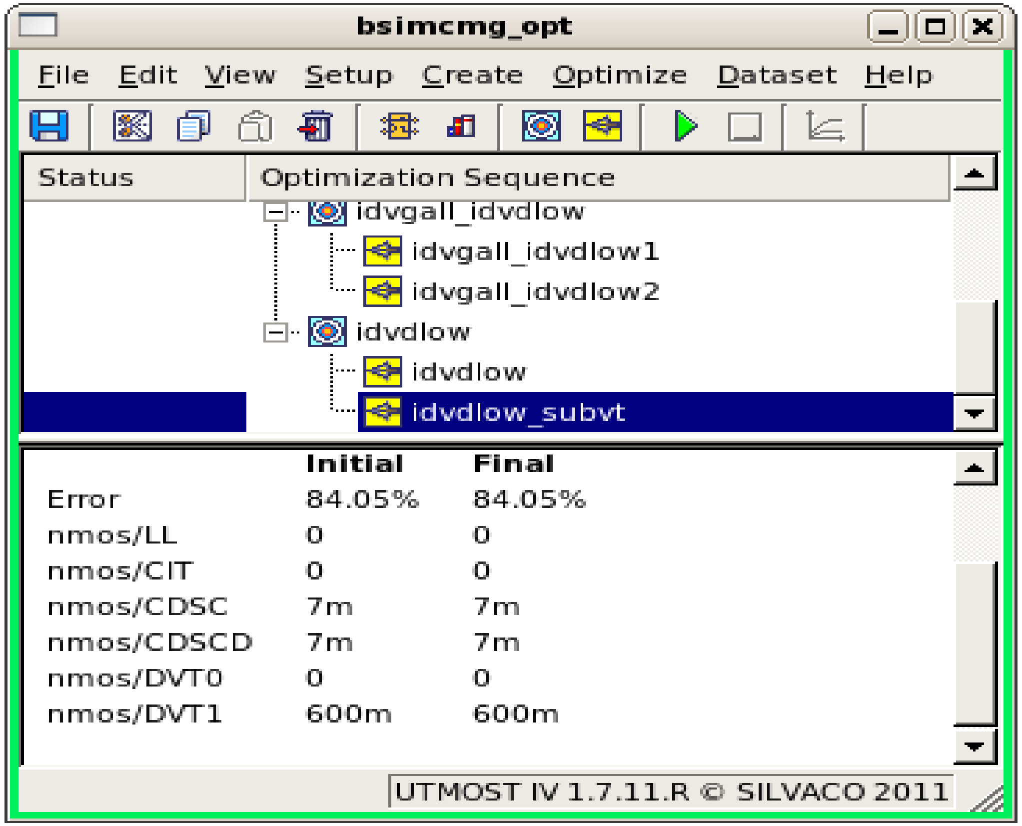
UTMOST IV BSIMCMG optimization sequence- idvd



- Target:
  - scaled length
  - idvd
- Optimizer:
  - Levenberg Marquardt

UTMOST IV BSIMCMG optimization sequence- idvd



- Target:
  - scaled length
  - idvd
- Optimizer:
  - Levenberg Marquardt

Basic flow of MOS model parameter optimization-1

Process parameters such as Tox should be provided.

1. **Cgg, Cgc / scaled geometry devices**

Capacitance model optimization

Include the geometry correction parameters. Maximum values of gate capacitances in the modern MOS models are a function of the gate area. Small device capacitance is much sensitive to the geometry correction terms.

2. **IdVg at the linear Vds / large geometry device**

Threshold & sub-threshold voltage region optimization

IdVg at the linear Vds of the reference (large) device can provide the basic device channel information. The step 1 and 2 should be combined when the capacitance model couples with the DC model.

3. **IdVg at the linear Vds / large geometry device**

Strong inversion region optimization

Mobility and resistance parameter optimization can lead to the better fitting of the threshold region due to the IdVg slope change. Then, the step 2 and 3 should be repeated, or combined.

Basic flow of MOS model parameter optimization-2

4. IdVg at the linear Vds / scaled geometry devices

Threshold, sub-threshold and strong inversion region optimizations for the scaled geometry.

All geometry scaling parameters should be optimized. The geometry correction terms which are independent of the gate capacitance (if exists) should be used. This step could be divided into the each regions for the decomposable models.

5. IdVd / scaled geometry devices — optional

The lowest Vgs region where the small drain current flows is necessary for the analog application.

No dedicated model parameter might exist. And the region demands the accurate threshold model expression.

6. IdVd / scaled geometry devices — optional

The gds at the high Vgs region should be optimized prior to the drain current optimization.

The step is optional when the drain current degradation at the high Vgs is prominent.

Basic flow of MOS model parameter optimization-3

7. IdVd at no body bias with IdVg at the linear and the saturation Vds/ scaled geometry devices

Saturation model parameter optimization

The saturation region IdVg could provide the adequate saturation model parameters only when the quasi-saturation effect is weak in IdVd. Otherwise, the linear region of IdVd with two IdVg characteristics should be used to get the initial saturation parameters under the fixed linear model parameters. Then, the linear and the saturation IdVd should be optimized with both the linear and saturation model parameters, i.e., the saturation model parameters are forced to find the initial values suitable for the linear region IdVd with no assistance of the linear model parameter optimization. The saturation IdVg gives the constraint. The previous steps to determine the linear model parameters should be reviewed when the initial saturation model parameters failed to provide the reasonable linear region IdVd.

8. IdVd / all geometry devices

Include the linear model parameters with care when the linear region IdVd needs the precise fit.

The previous step 7 should provide the good IdVd fit. This step is to get the best possible model.

9. All temperature characteristics / all geometry devices

Temperature model optimization

Check the temperature model flag (if exists) before the execution.

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Summary

•BSIMCMG model was reviewed briefly.

•UTMOST IV BSIMCMG parameter optimization sequence was explained.

•Basic flow of MOS model parameter optimization which is suitable for the modern MOS models was summarized.